

# LCFC Confidential


## BMWC1&C2 M/B Schematics Document

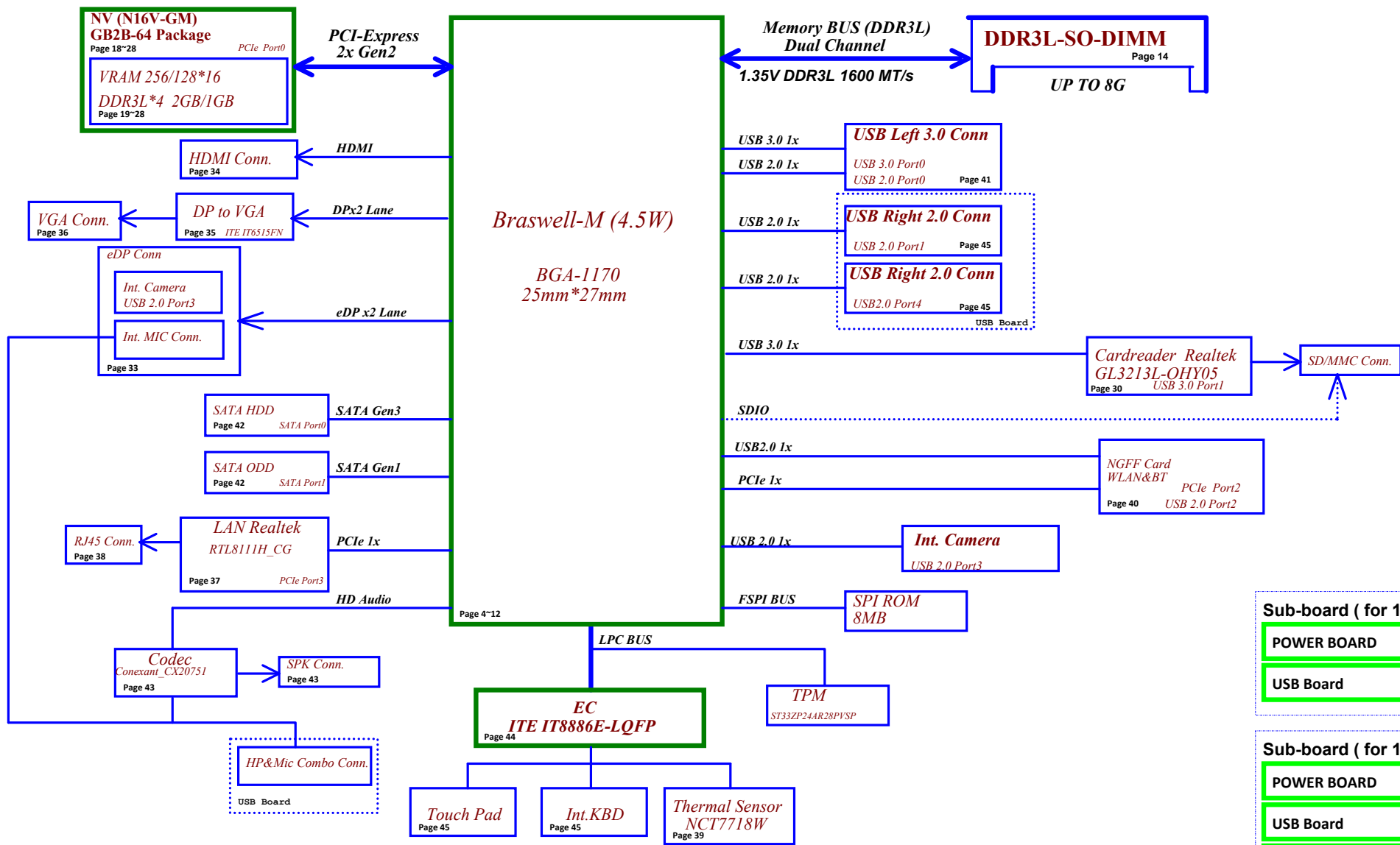
NM-A471 REV:0.4

Intel Braswell M-Processor with DDRIIIL + NV (N16V-GM) GPU

2015-03-23

REV: 0.4

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2014/09/24	Deciphered Date	2015/03/23	Cover Page			
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Date: Tuesday, April 07, 2015				Sheet 1 of 60			



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	Block Diagram	
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Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane \ State	B+	+3VALW	+3VALW_SOC +1.0VALW	+1.35V	+5VS +3VS +1.5VS  +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	EC +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_100xb(reserve)	DDR DIMMA	1010 000Xb
Charger	need to update	VGA	0x9E(base on NV default)	Wlan	Rsvd
				TP	need to update

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB Port (Left Side)
	1	USB3.0 Card Reader
USB 2.0	0	USB Port (Left Side)
	1	USB Port (Right Side)
	2	BT
	3	Camera
	4	USB Port (Right Side)
USB HUB	1	
	2	
	3	
	4	

BOM Structure Table

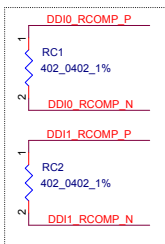
BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	GPU Part
UMA@	UMA SKU ID part
14@	For 14" part
15@	For 15" part
100M@	100M LAN part
N15SGT@	N15SGT Part
N15VGM@	N15GSM Part
GIGA@	GIGA LAN Part
GC6@	GPU GC6 Part
TS@	Touch Screen part
RANKA@	GPU VRAM RANKA PART
RANKB@	GPU VRAM RANKB PART
ME@	Connector
CD@	COST DOWN
@	Not stuff
H4T@	Hynix VRAM Part
M4T@	Micron VRAM Part
S4T@@	Samsung VRAM Part

PCIE PORT LIST

Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI



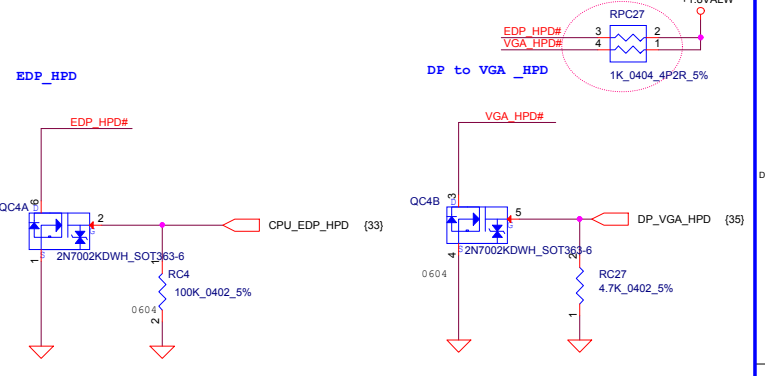
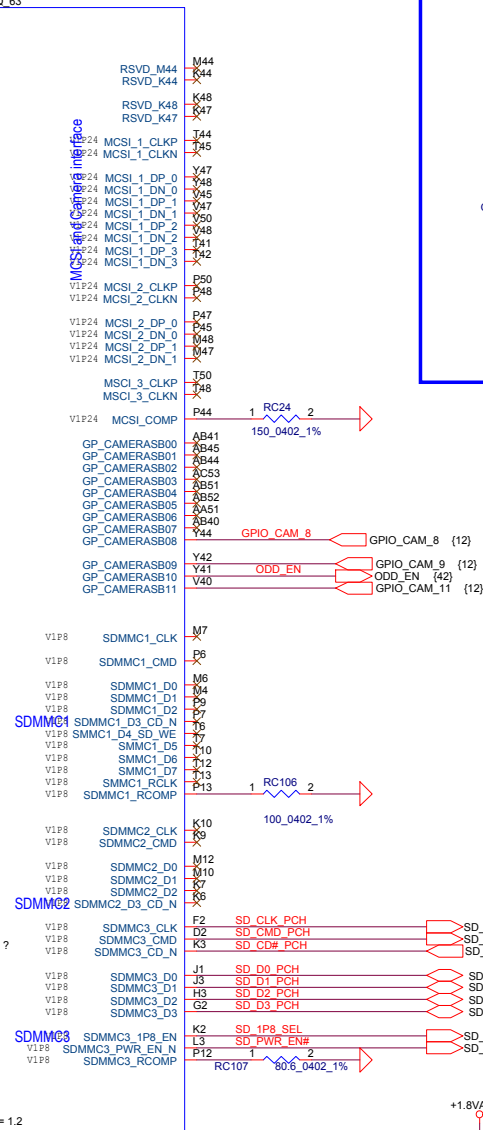
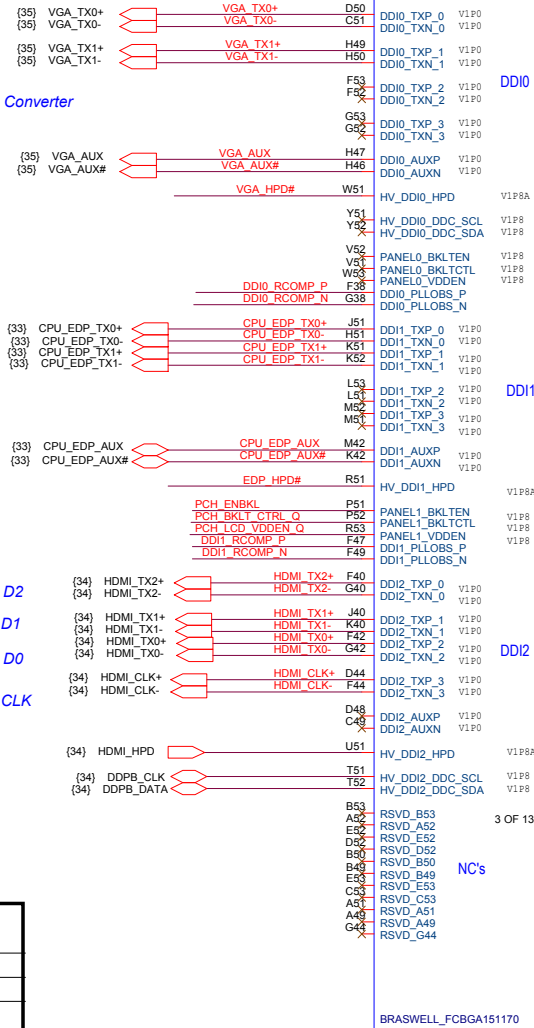
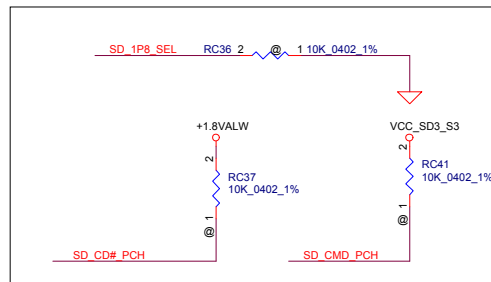
DP TO VGA Converter

EDP

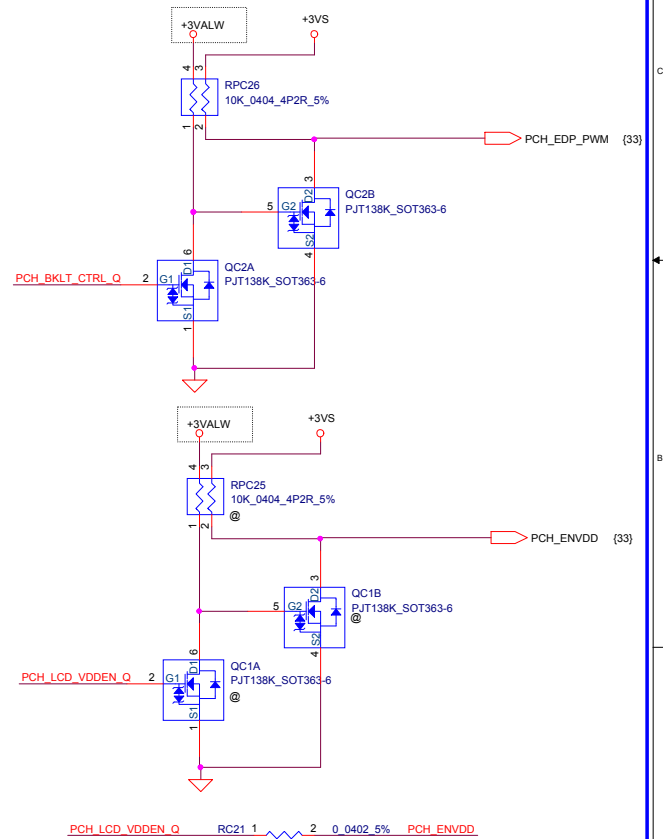
HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

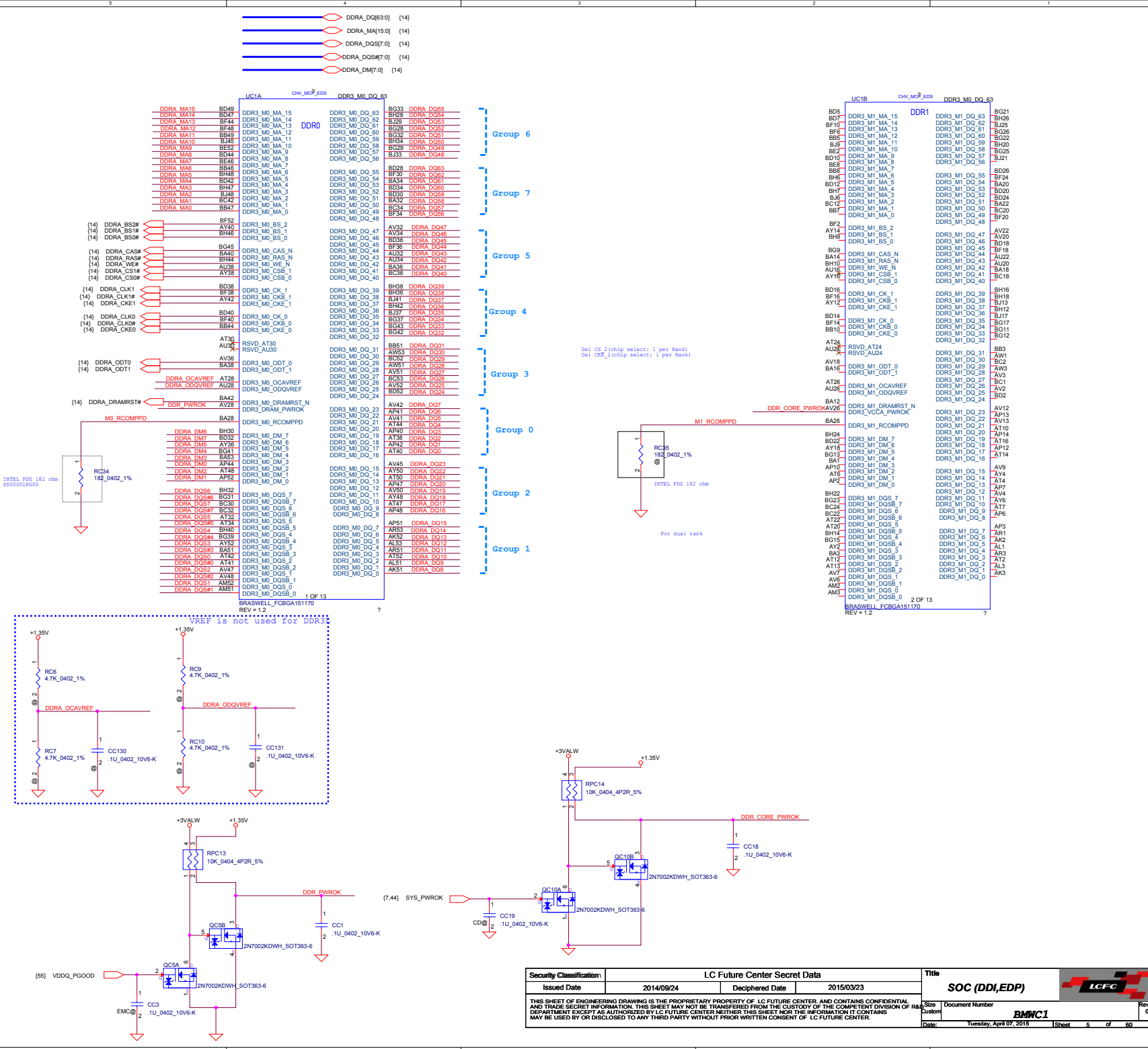
## DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

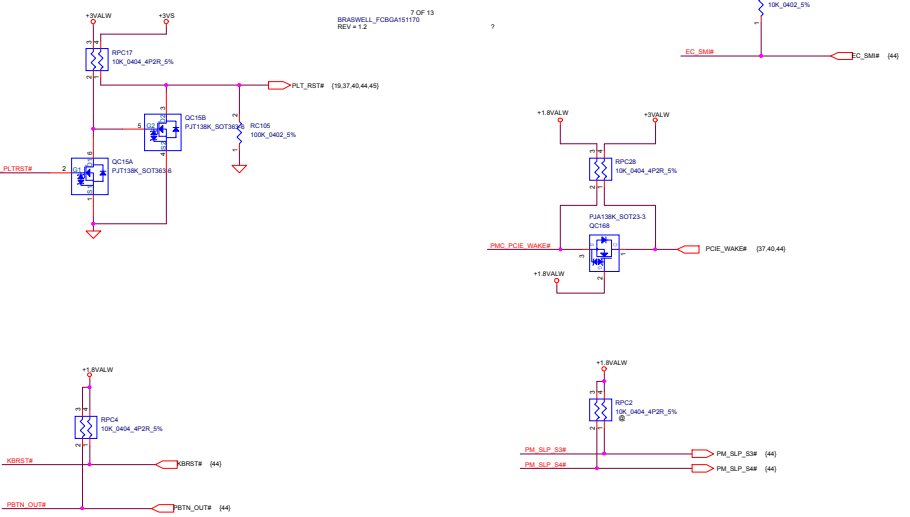
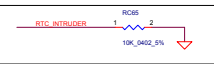
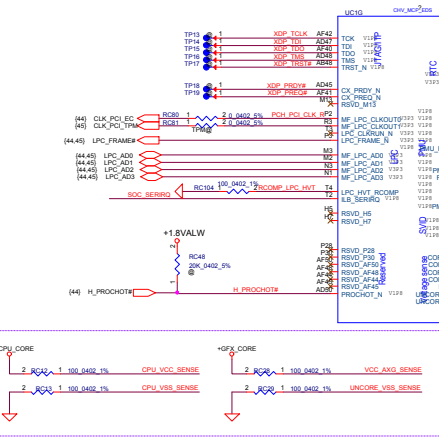
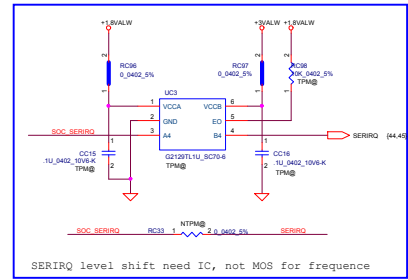


PCH\_ENBK\_L can direct connect to EC for costdown

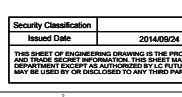
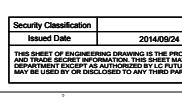
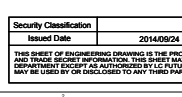
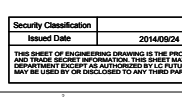
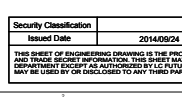
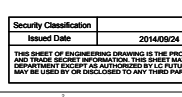
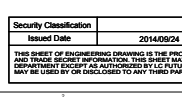
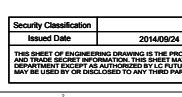
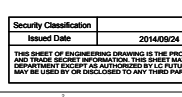
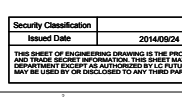
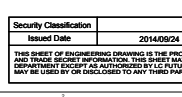
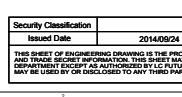
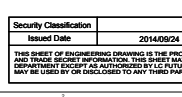
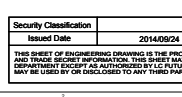
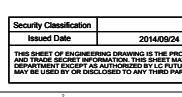
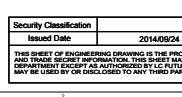
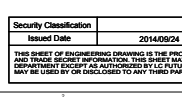
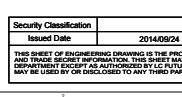
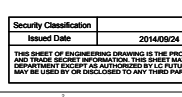
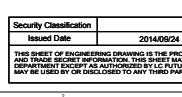
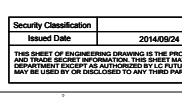
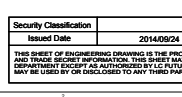
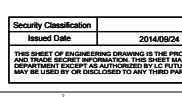
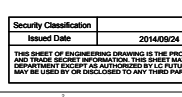
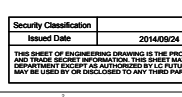
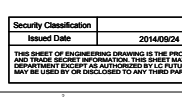
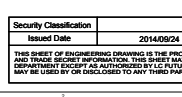
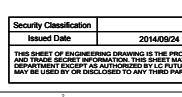
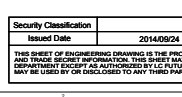
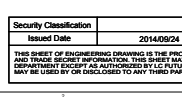
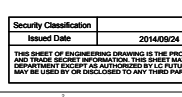
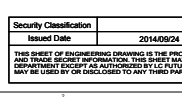
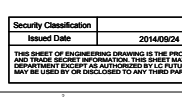
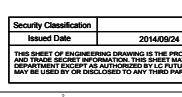
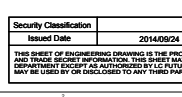
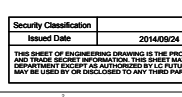
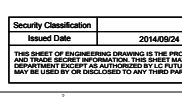
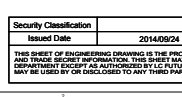
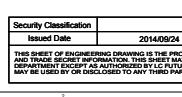
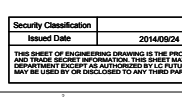
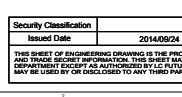
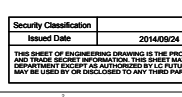
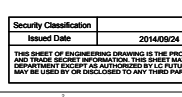
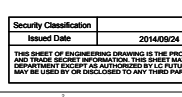
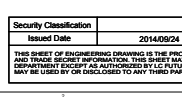
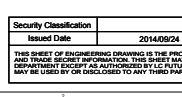
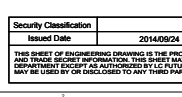
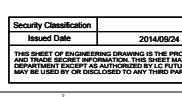
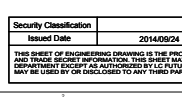
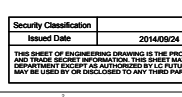
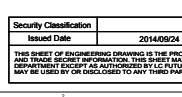
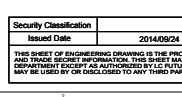
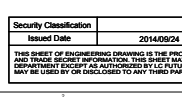
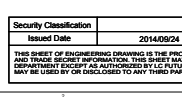
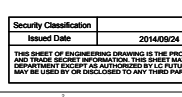
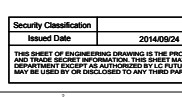
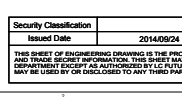
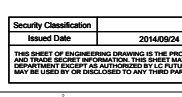
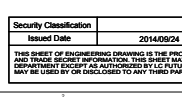
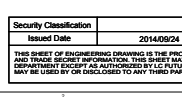
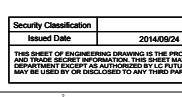
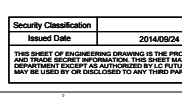
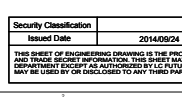
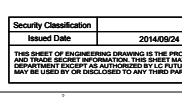
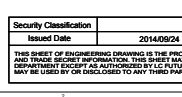
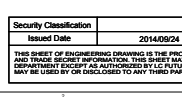
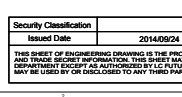
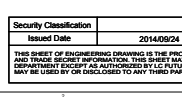
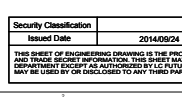
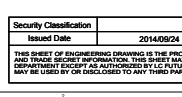
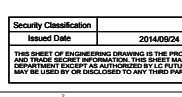
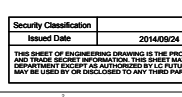
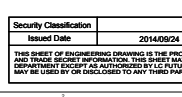
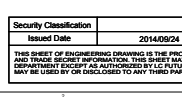
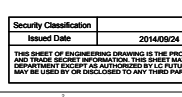
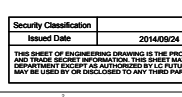
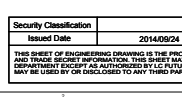
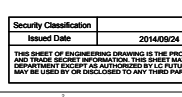
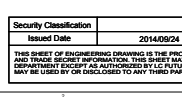
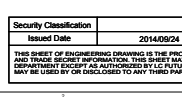
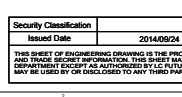
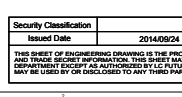
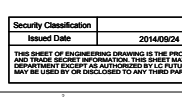
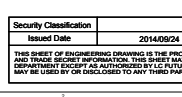
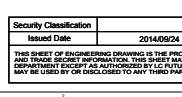
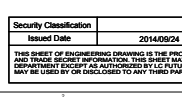
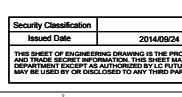
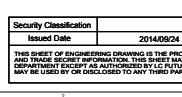
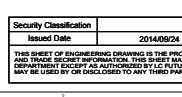
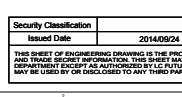
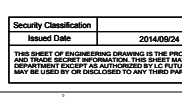
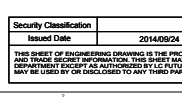
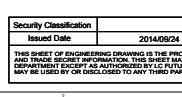
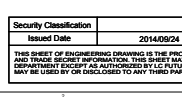
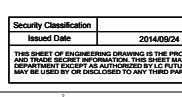
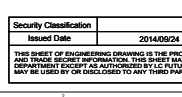
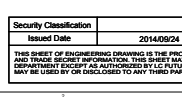
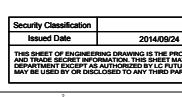
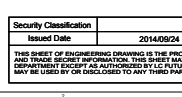
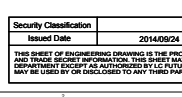
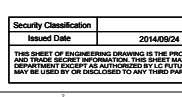
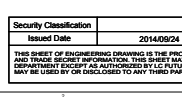
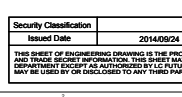
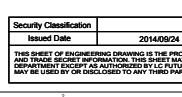
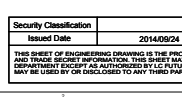
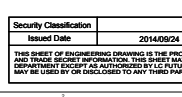
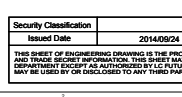
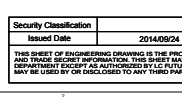
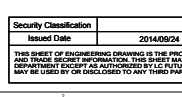
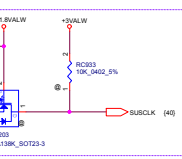
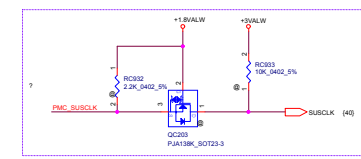
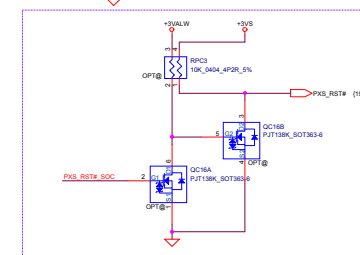
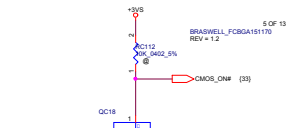
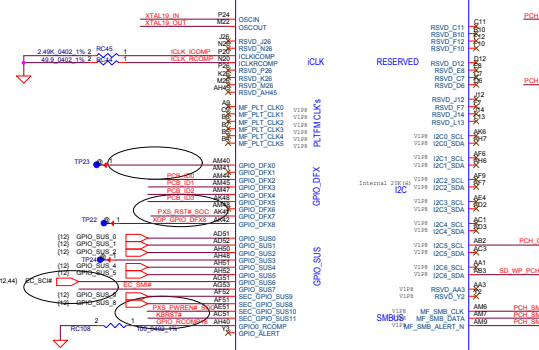
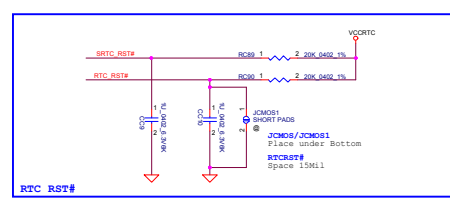
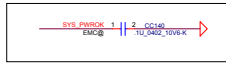
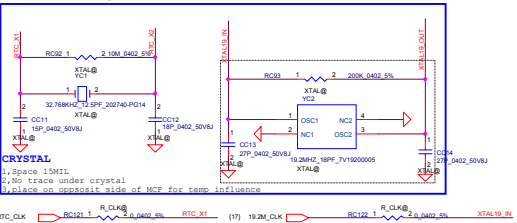


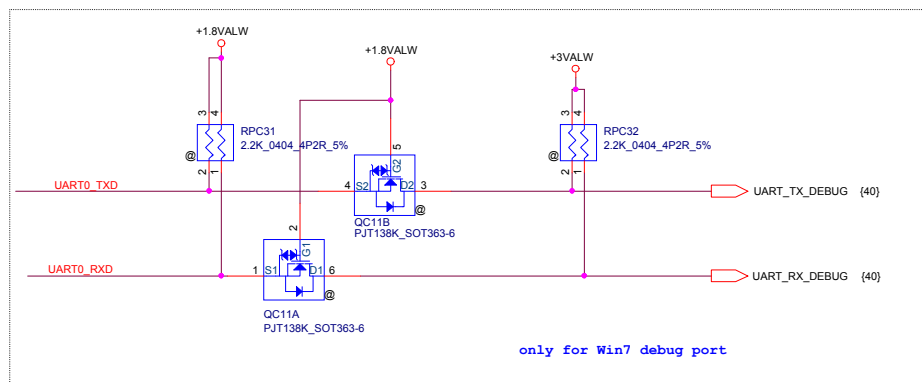
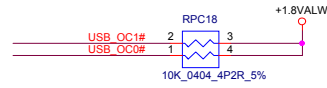
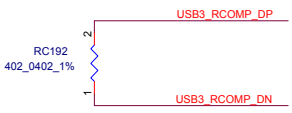
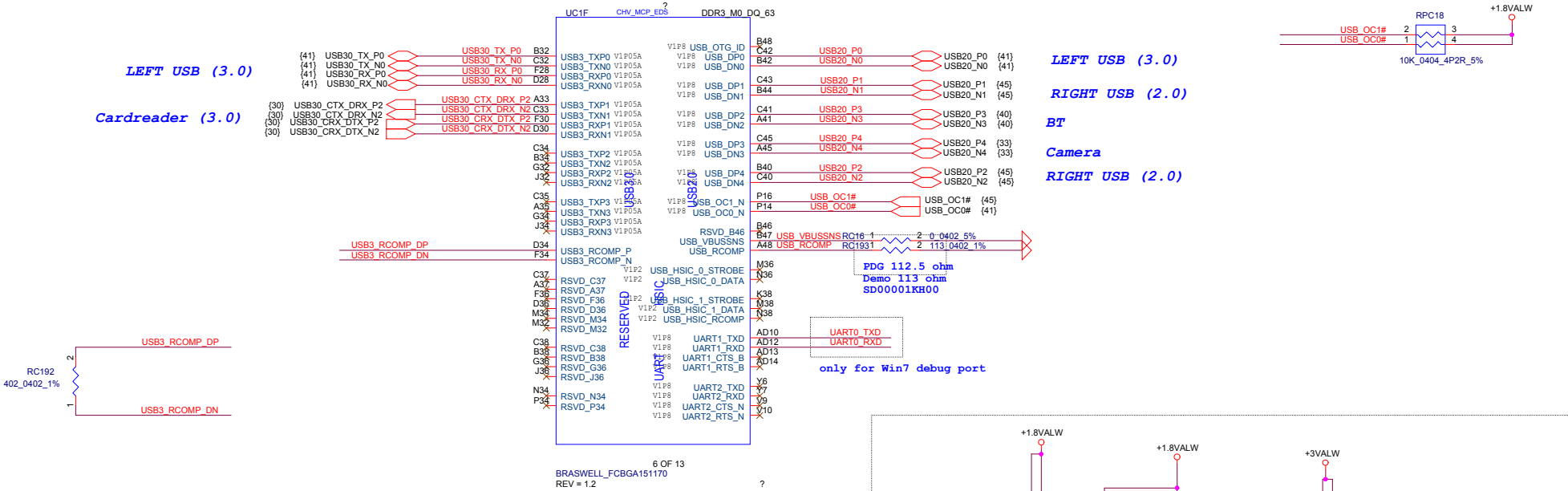






32.768K need change to SJ100001M00,  
as intel SDS New Request





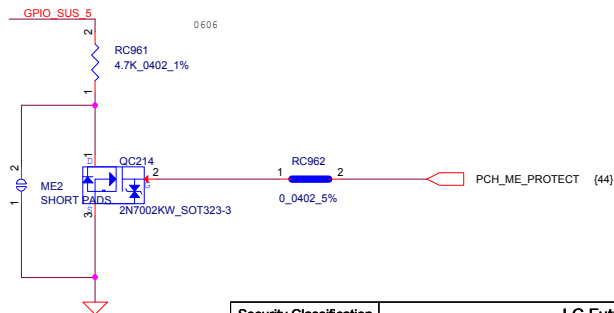
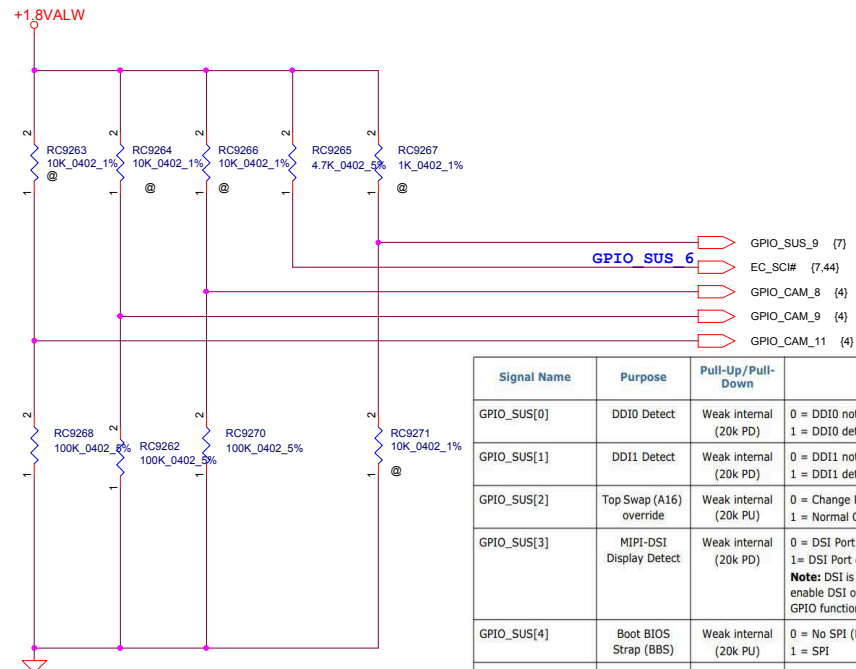
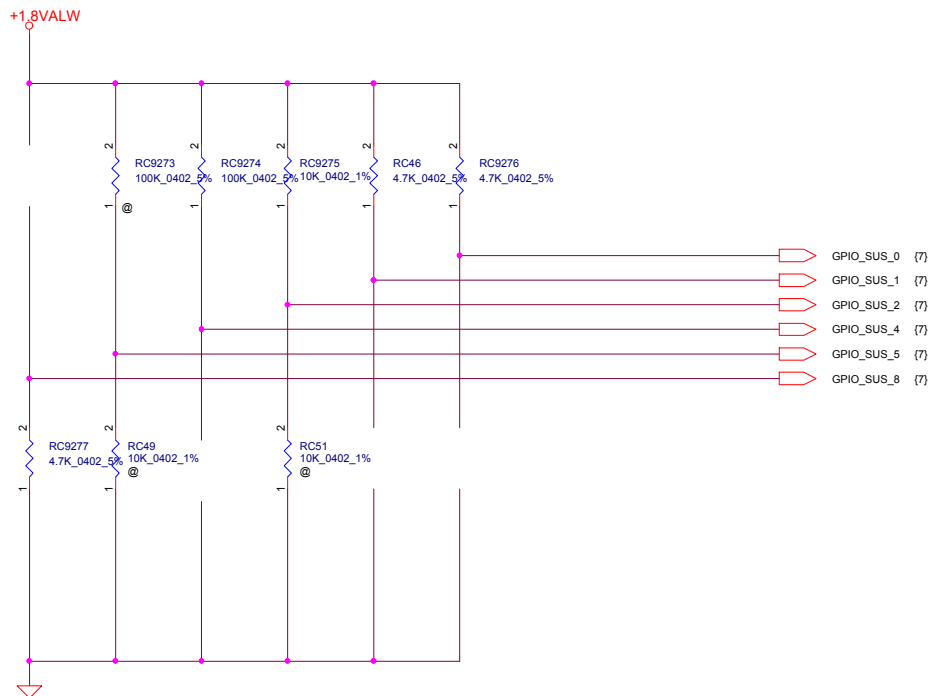






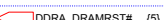



Hardware STRAPS  
(Follow up CRB)



Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected <b>Note:</b> DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1 = Normal Operation <b>Note:</b> This strap <b>MUST</b> be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

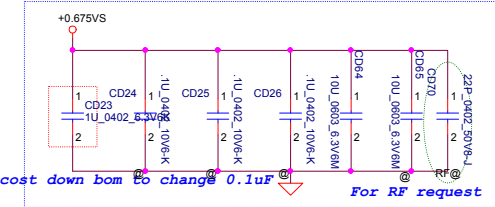
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		Sheet	12 of 60

**DDR3 SO-DIMM A**

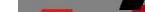
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(10uF\_0603\_6.3V)\*8  
(0.1uF\_402\_10V)\*4




cost down bom to change 0.1uF

Title		<b>DDRIII SO-DIMM A</b>			
Size	Document Number	<b>BMWC1</b>		Rev	0.4
Custom					
Date:	Tuesday, April 07, 2015	Sheet	14	of	60

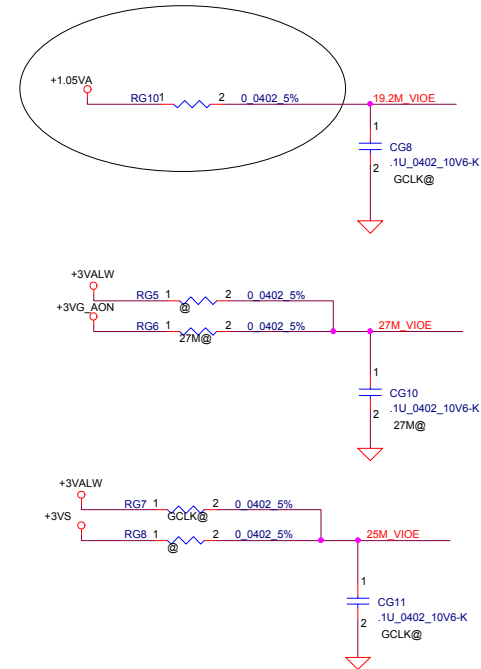
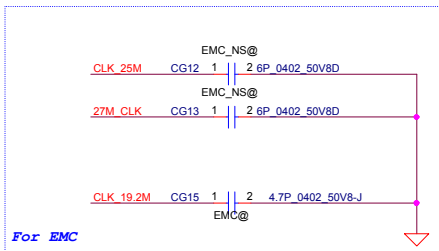
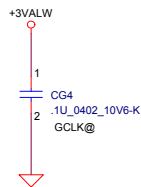
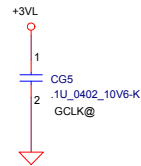
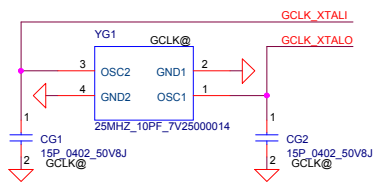
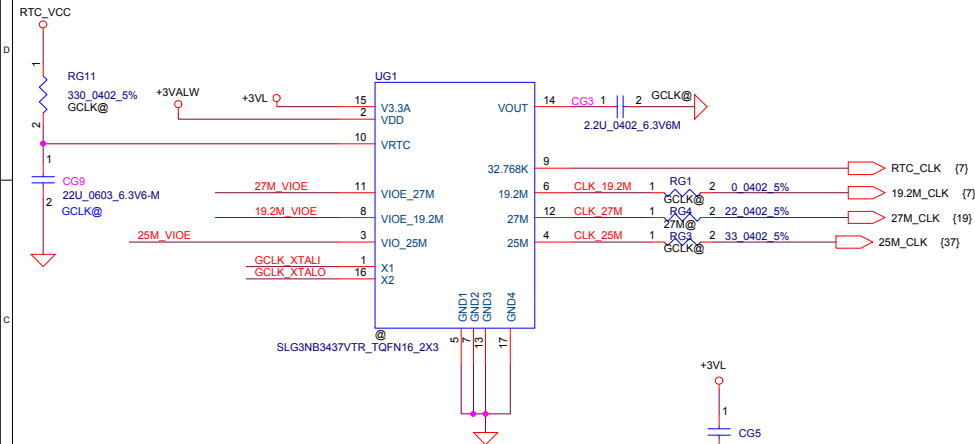
Swap Table


Pin Number	Pin Name	Net Name
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7	DQ1	DDR8_DQ23
15	DQ2	DDR8_DQ18
17	DQ3	DDR8_DQ21
4	DQ4	DDR8_DQ16
6	DQ5	DDR8_DQ22
16	DQ6	DDR8_DQ19
18	DQ7	DDR8_DQ20
10	DQS#0	DDR8_DQS#2
12	DQS0	DDR8_DQS2
21	DQ8	DDR8_DQ3
23	DQ9	DDR8_DQ5
33	DQ10	DDR8_DQ6
35	DQ11	DDR8_DQ1
22	DQ12	DDR8_DQ2
24	DQ13	DDR8_DQ4
34	DQ14	DDR8_DQ0
36	DQ15	DDR8_DQ7
27	DQS#1	DDR8_DQS#0
29	DQS1	DDR8_DQS0
39	DQ16	DDR8_DQ8
41	DQ17	DDR8_DQ10
51	DQ18	DDR8_DQ14
53	DQ19	DDR8_DQ15
40	DQ20	DDR8_DQ13
42	DQ21	DDR8_DQ12
50	DQ22	DDR8_DQ9
52	DQ23	DDR8_DQ11
45	DQS#2	DDR8_DQS#1
47	DQS2	DDR8_DQS1
57	DQ24	DDR8_DQ27
59	DQ25	DDR8_DQ26
67	DQ26	DDR8_DQ28
69	DQ27	DDR8_DQ24
56	DQ28	DDR8_DQ31
58	DQ29	DDR8_DQ30
68	DQ30	DDR8_DQ29
70	DQ31	DDR8_DQ25
62	DQS#3	DDR8_DQS#3
64	DQS3	DDR8_DQS3
129	DQ32	DDR8_DQ33
131	DQ33	DDR8_DQ36
141	DQ34	DDR8_DQ39
143	DQ35	DDR8_DQ38
130	DQ36	DDR8_DQ37
132	DQ37	DDR8_DQ32
140	DQ38	DDR8_DQ35
142	DQ39	DDR8_DQ34
135	DQS#4	DDR8_DQS#4
137	DQS4	DDR8_DQS4
147	DQ40	DDR8_DQ40
149	DQ41	DDR8_DQ43
157	DQ42	DDR8_DQ42
159	DQ43	DDR8_DQ44
146	DQ44	DDR8_DQ45
148	DQ45	DDR8_DQ41
158	DQ46	DDR8_DQ46
160	DQ47	DDR8_DQ47
152	DQS#5	DDR8_DQS#5
154	DQS5	DDR8_DQS5
163	DQ48	DDR8_DQ52
165	DQ49	DDR8_DQ51
175	DQ50	DDR8_DQ50
177	DQ51	DDR8_DQ48
164	DQ52	DDR8_DQ49
166	DQ53	DDR8_DQ53
174	DQ54	DDR8_DQ54
176	DQ55	DDR8_DQ55
169	DQS#6	DDR8_DQS#6
171	DQS6	DDR8_DQS6
181	DQ56	DDR8_DQ62
183	DQ57	DDR8_DQ57
191	DQ58	DDR8_DQ59
193	DQ59	DDR8_DQ63
180	DQ60	DDR8_DQ56
182	DQ61	DDR8_DQ61
192	DQ62	DDR8_DQ58
194	DQ63	DDR8_DQ60
186	DQS#7	DDR8_DQS#7
188	DQS7	DDR8_DQS7

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3437:SA000078V00; 3436:SA000078X00



Security Classification		LC Future Center Secret Data		Title			Rev 0.4	
Issued Date		2014/09/24	Deciphered Date		2015/03/23			Blank
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Date:		Tuesday, April 07, 2015		Sheet		17	of 60	

N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

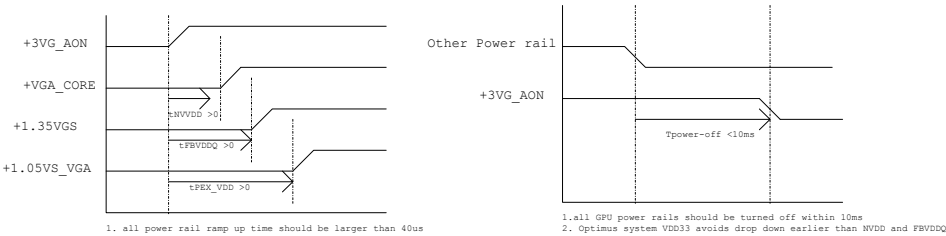
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (s)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

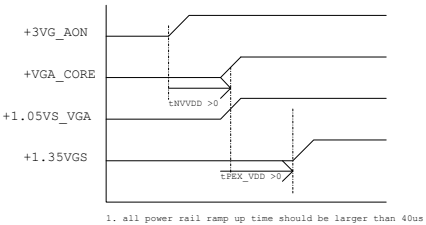
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved (keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS				
STRAP2	+3VGS	Reserved (keep pull-up and pull-down footprint and not stuff by default)			
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



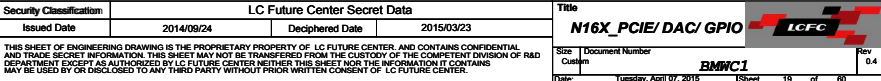
N15S-GT Power Sequence

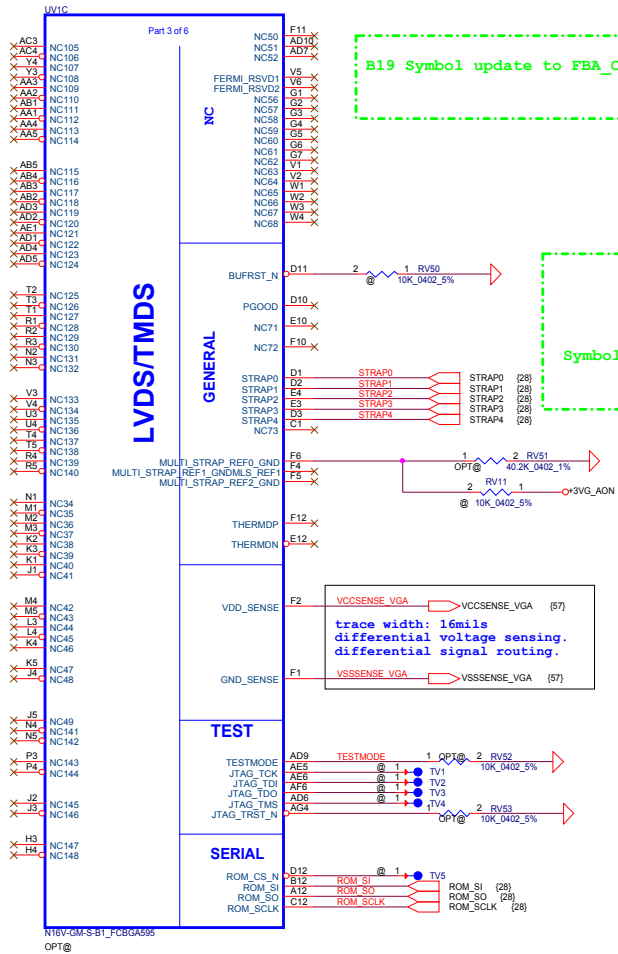


N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED







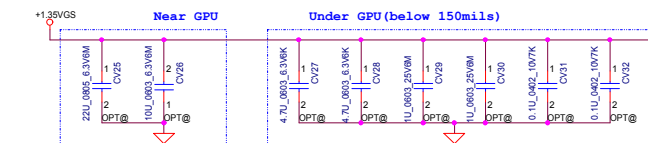
B19 Symbol update to FBA\_CMD32

Symbol update to GPIO8

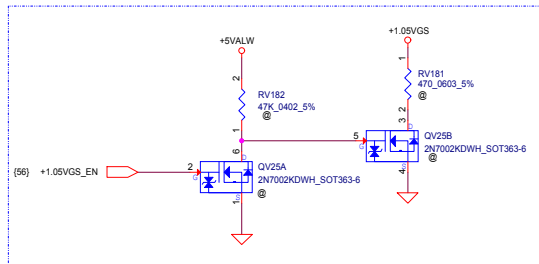
VCCSENSE\_VGA → VCCSENSE\_VGA (57)

trace width: 16mils  
differential voltage sensing.  
differential signal routing.

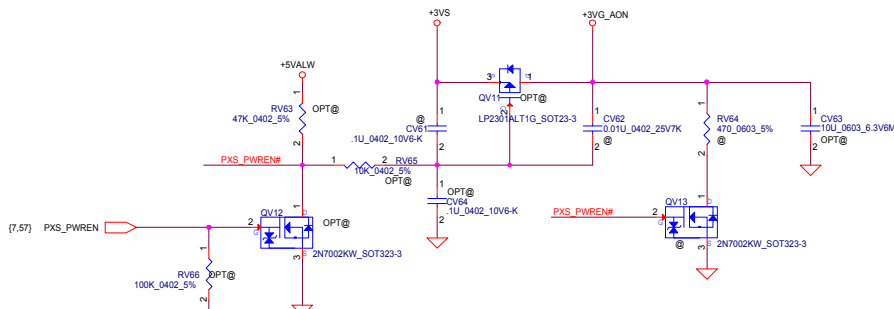
VSSSENSE\_VGA → VSSSENSE\_VGA (57)



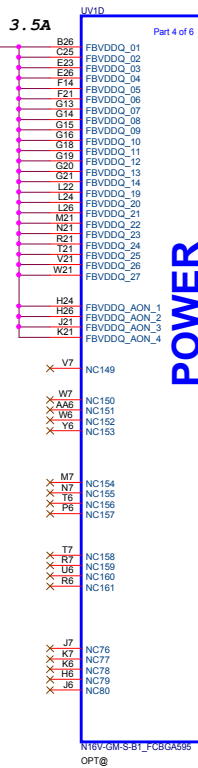
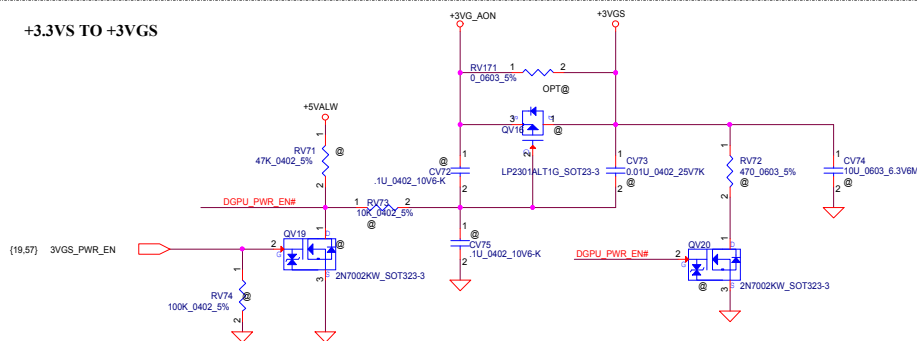
Symbol update to FBVDDQ\_AON  
H24/H26/J21/K21



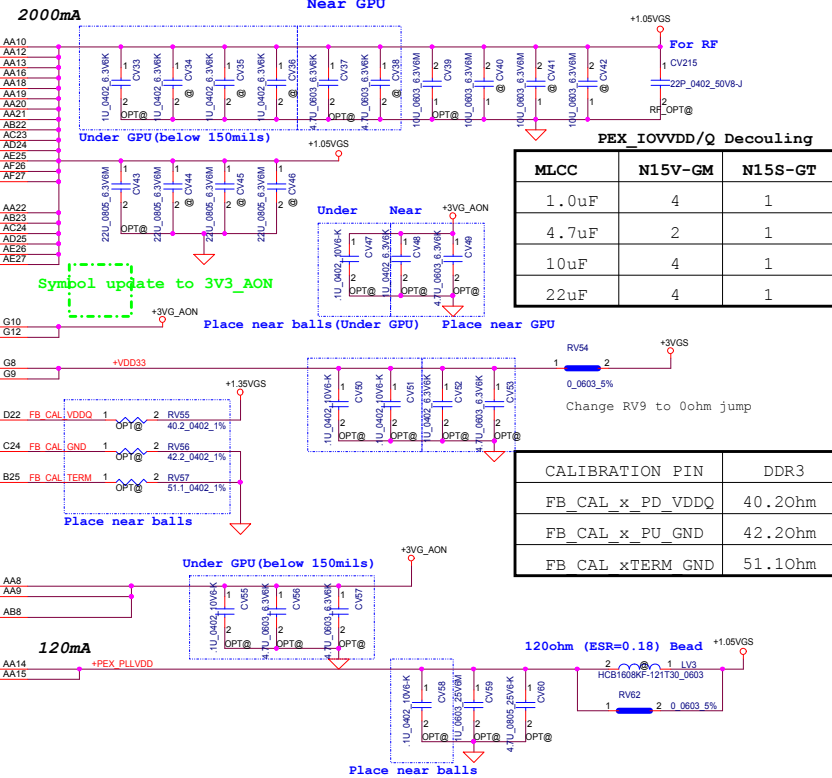
**+3VGS to +3VGS\_AON**



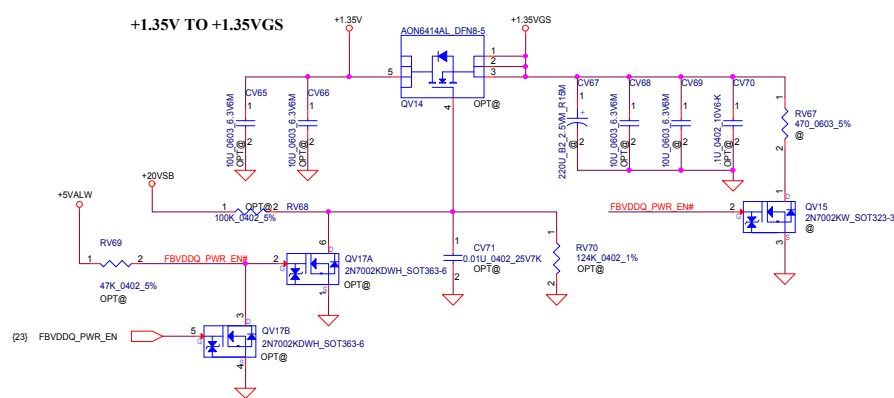
**+3VGS to +3VGS**

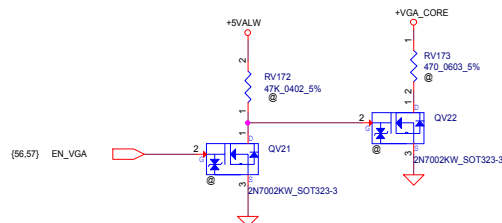
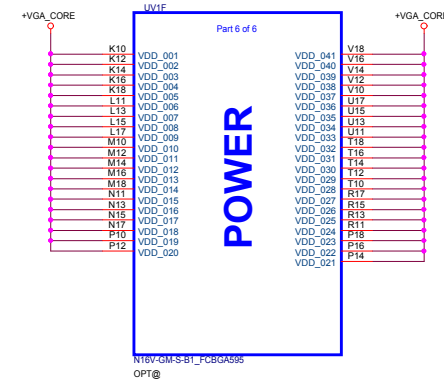
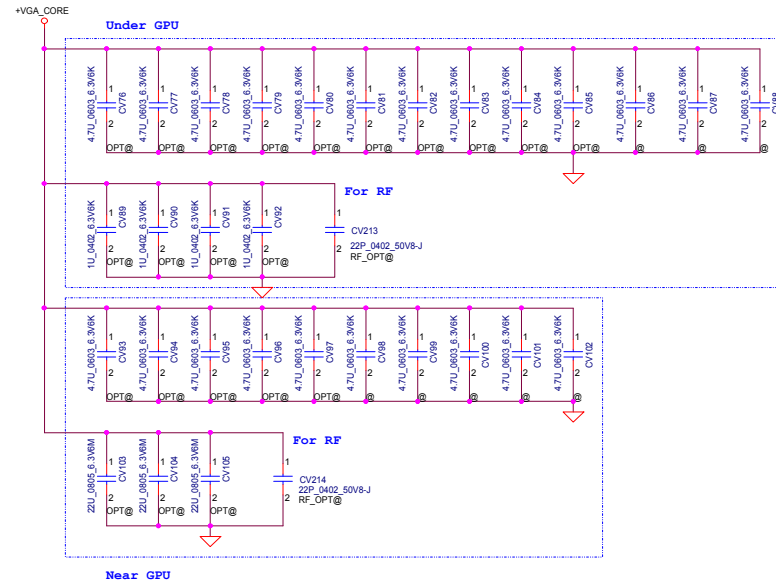
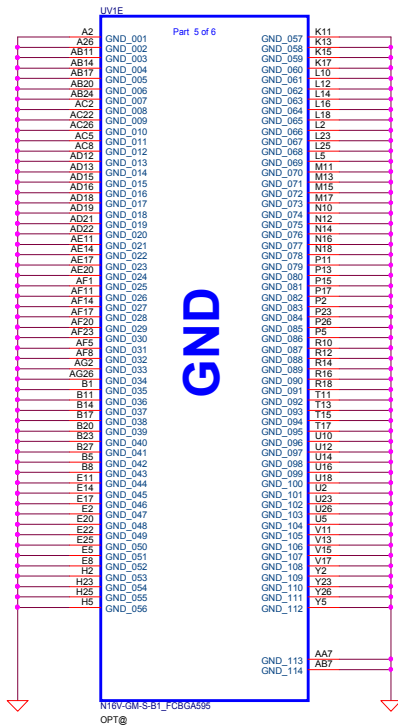


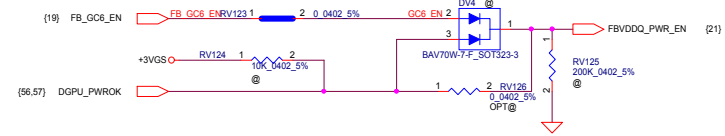
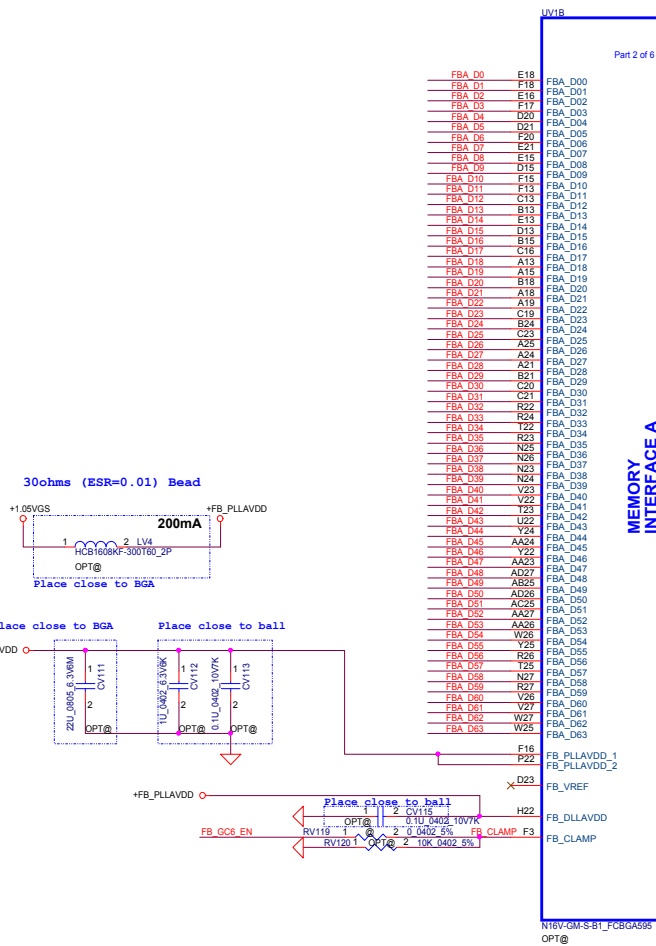
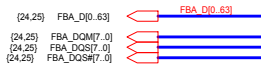
## POWER



**+1.35V to +1.35VGS**



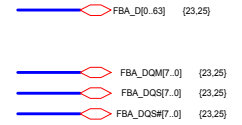
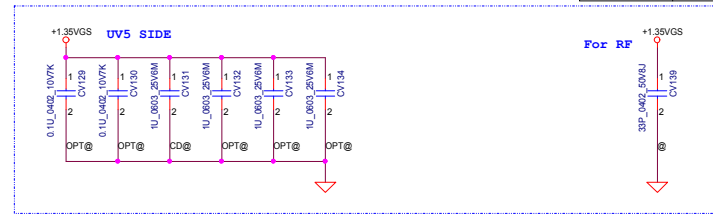
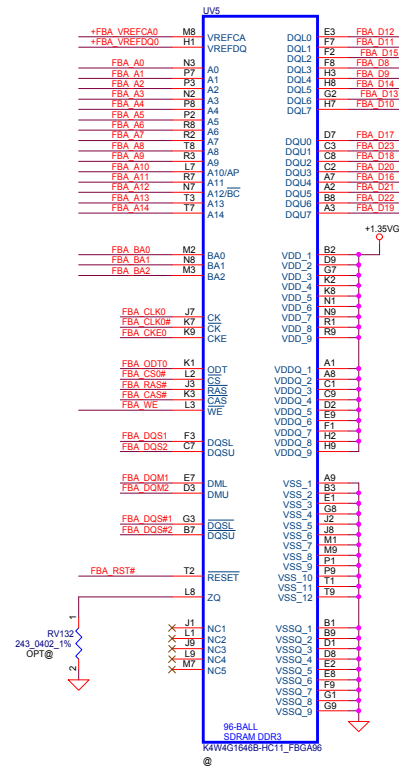
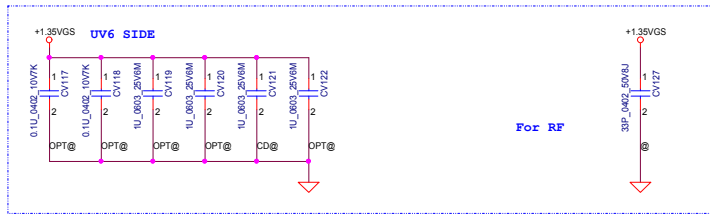
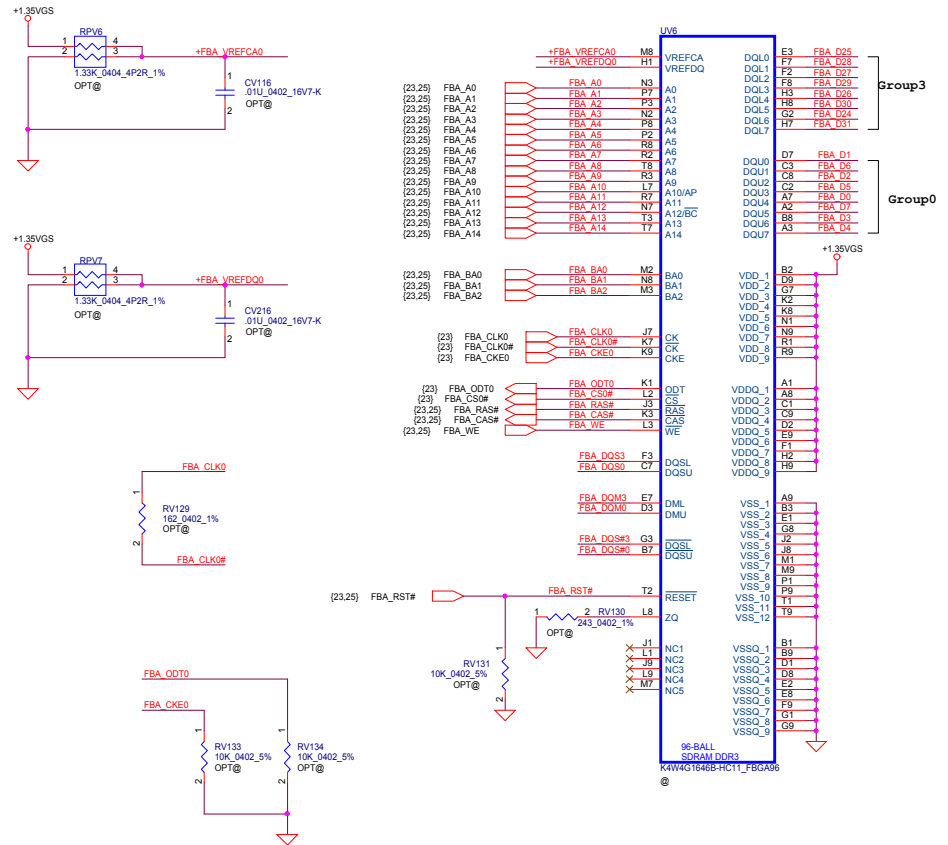




CMD mapping mod Mode D

		Rank0	
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16		CS1#	
FBx_CMD17			
FBx_CMD18		ODT1	
FBx_CMD19		CKE1	
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		

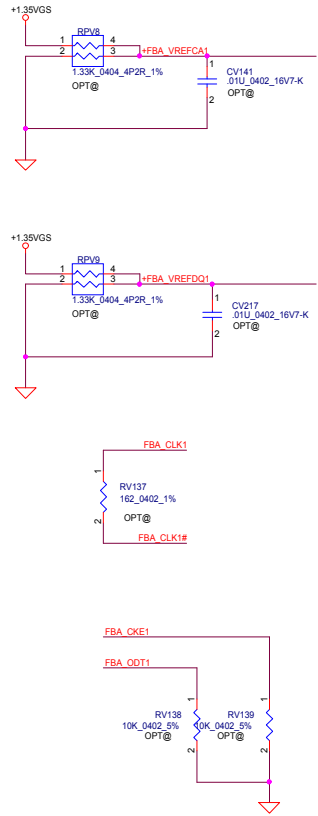
at least 16 mils width(optimal)  
20 mils spacing to other signals /planes



### CMD mapping mod Mode D

Rank0		Rank0	
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16	CS1#		
FBx_CMD17			
FBx_CMD18		ODT1	
FBx_CMD19		CKE1	
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		

at least 16 mils width(optimal)  
20 mils spacing to other signals /planes



FBA\_D[0..63] (23,24)

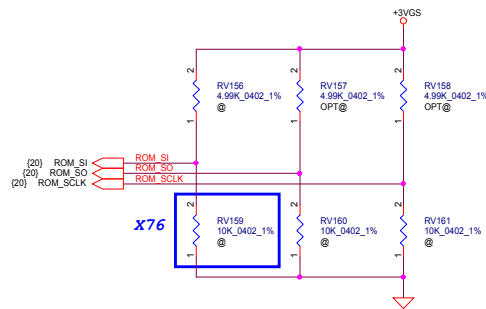
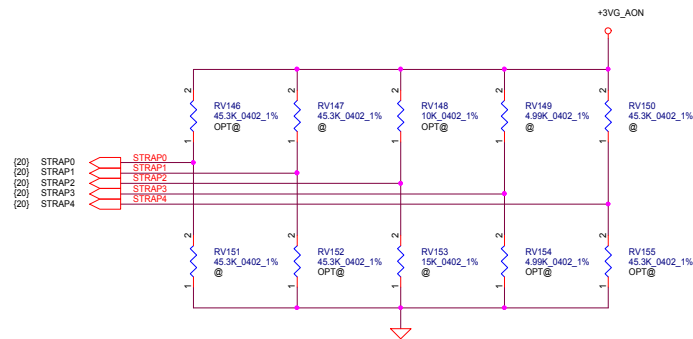
FBA\_DQM[7..0] (23,24)

FBA\_DQS[7..0] (23,24)

FBA\_DQS[7..0] (23,24)

### CMD mapping mod Mode D

Rank0		Rank1	
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16		CS1#	
FBx_CMD17			
FBx_CMD18		ODT1	
FBx_CMD19		CKE1	
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K SD03449918J	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K SD03449928J	1100	0100
30.1K SD03449928J	1101	0101
34.8K SD03449928J	1110	0110
45.3K SD03449928J	1111	0111

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

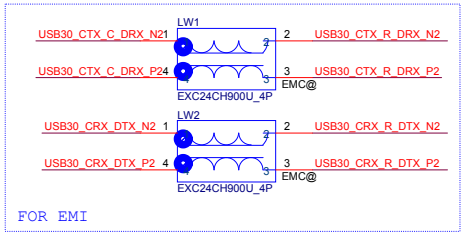
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76											
GPU	FB Memory (DDR3L)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N16V-GM	Hynix 900MHz	H5TC4G63AFR-11C	0xE	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K	
		256M x 16 0xE	PU 34.8K								
	Micron 900MHz	MT41J256M16HA-093G:E	0xD								PU 30.1K
		256M x 16 0xD									
	Hynix 900MHz	H5TC2G63FFR-11C	0xB								PU 20K
		128M x 16 0xB									
	Micron 900MHz	MT41J128M16JT-093G	0x8								PU 4.99K
		128M x 16 0x8									
	Samsung 900MHz	K4W2G1646Q-BC1A	0x7								PD 45.3K
		128M x 16 0x7									

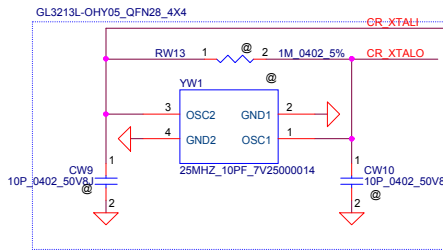
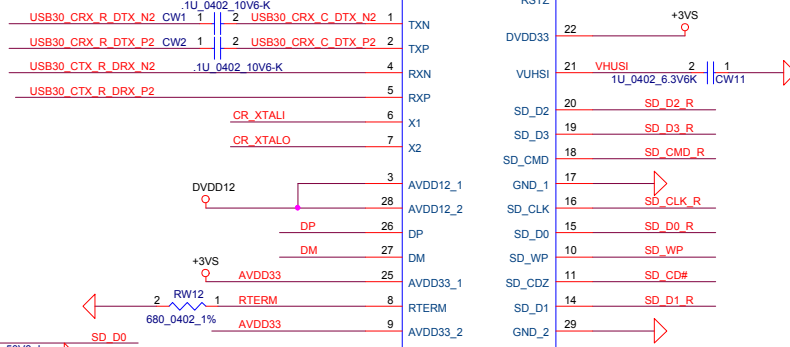
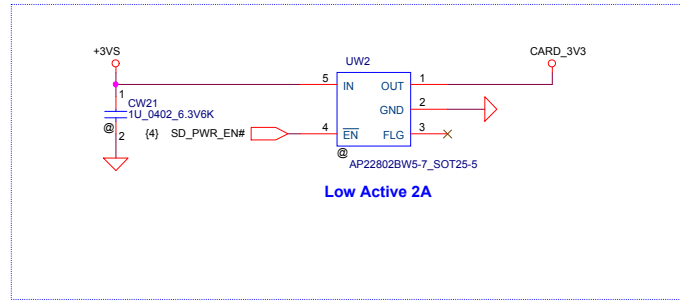
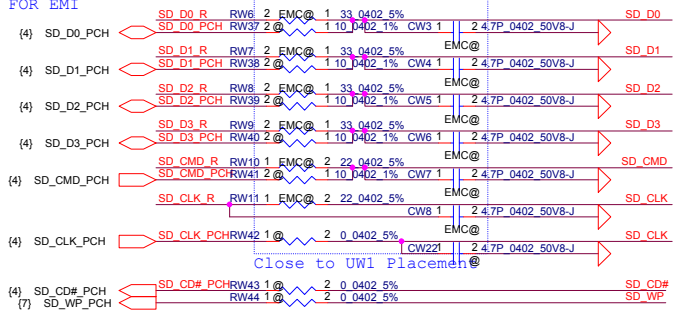
VRAM	X76	VRAM P/N
Samsung	X7606012101	SA00005SH40
Micron	X7606012001	SA00005M120
Hynix	X7606012002	SA00005VS00



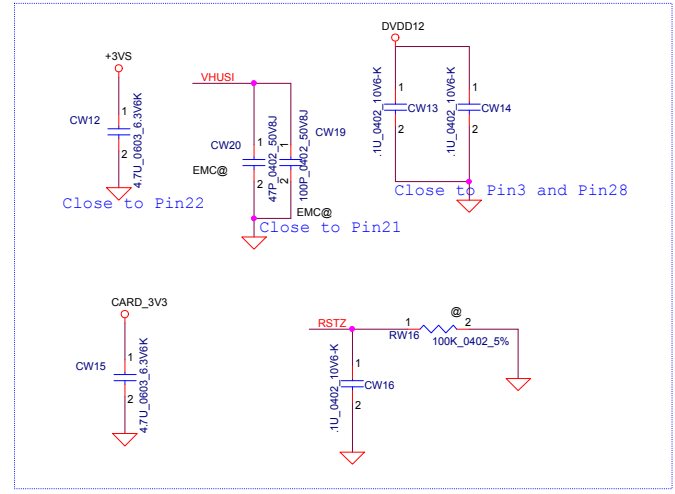
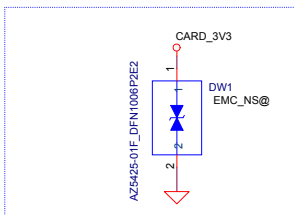
(8) USB30\_CTX\_DRX\_N2 1U\_0402\_10V6-K CW25 1 2 USB30\_CTX\_C\_DRX\_N2 1 RW1 @ 2 0.0402\_5% USB30\_CTX\_R\_DRX\_N2  
(8) USB30\_CTX\_DRX\_P2 1U\_0402\_10V6-K CW26 1 2 USB30\_CTX\_C\_DRX\_P2 1 RW2 @ 2 0.0402\_5% USB30\_CTX\_R\_DRX\_P2  
(8) USB30\_CRX\_DTX\_N2 1 USB30\_CRX\_DTX\_N2 RW3 1 @ 2 0.0402\_5% USB30\_CRX\_R\_DTX\_N2  
(8) USB30\_CRX\_DTX\_P2 1 USB30\_CRX\_DTX\_P2 RW4 1 @ 2 0.0402\_5% USB30\_CRX\_R\_DTX\_P2



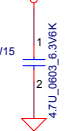
FOR EMI



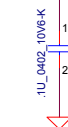
FOR ESD Close to Connector



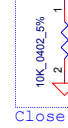
CARD\_3V3



RSTZ



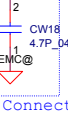
CARD\_3V3



RSTZ



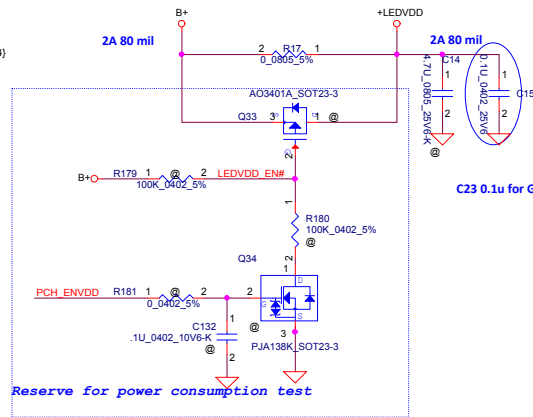
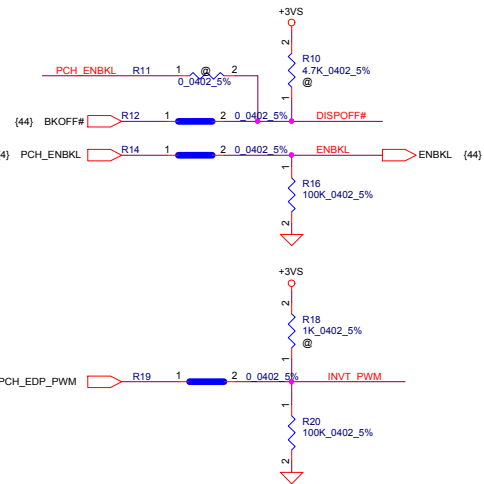
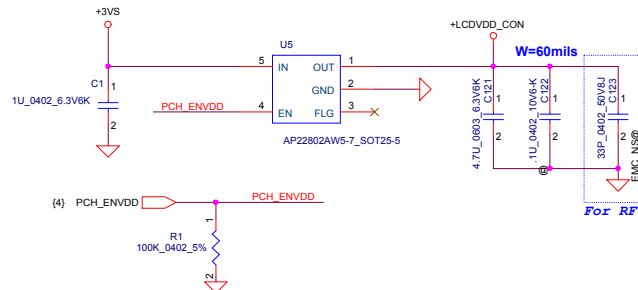
SD / MMC



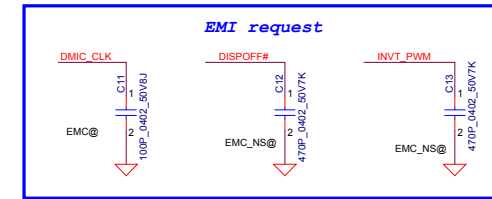
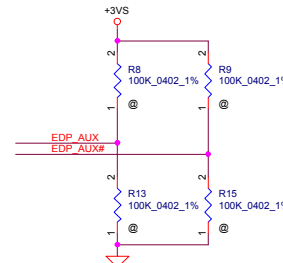
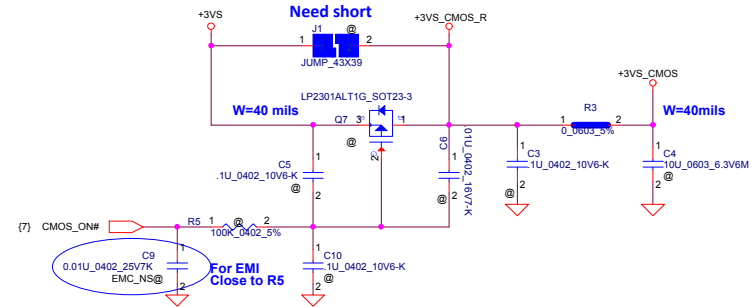
Security Classification	LC Future Center Secret Data		Title	Cardreader	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	Size	Document Number
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				Date	Tuesday, April 07, 2015
				Sheet	30 of 59
				Rev	0.4

# LCD POWER CIRCUIT

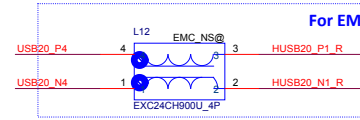
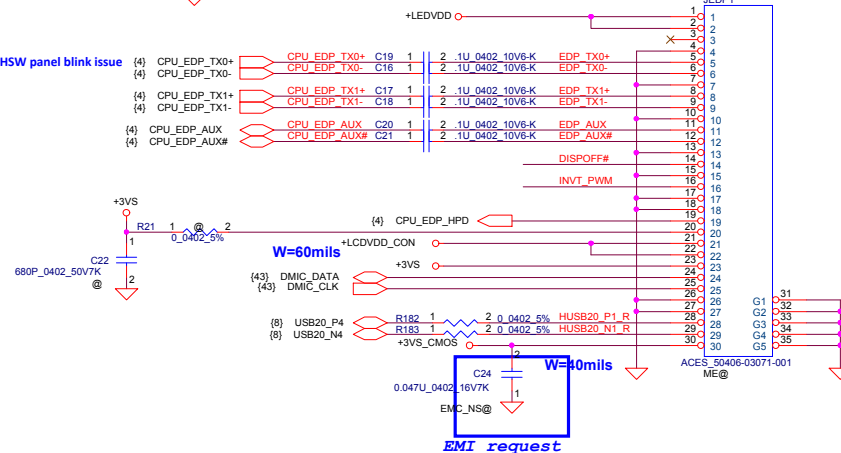
W=60mils

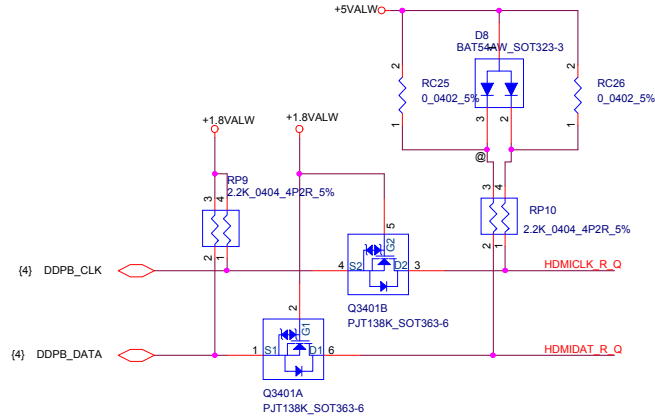
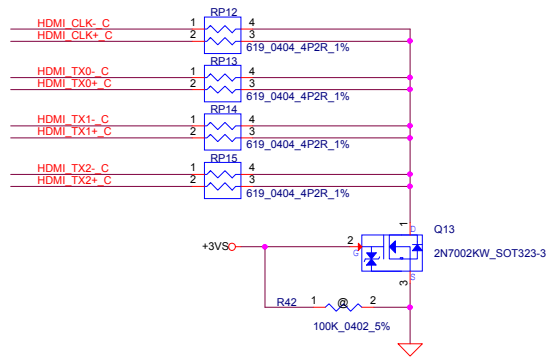
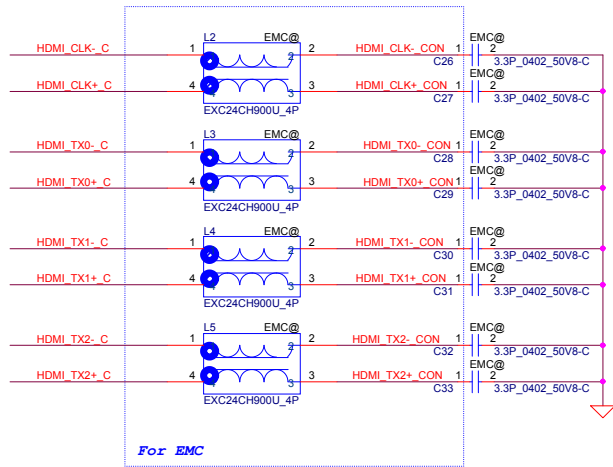


# CMOS Camera

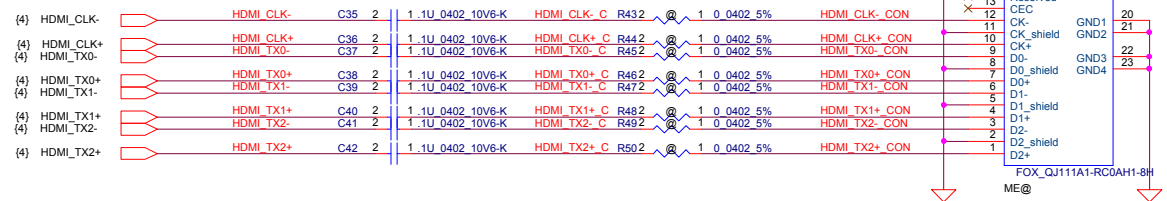
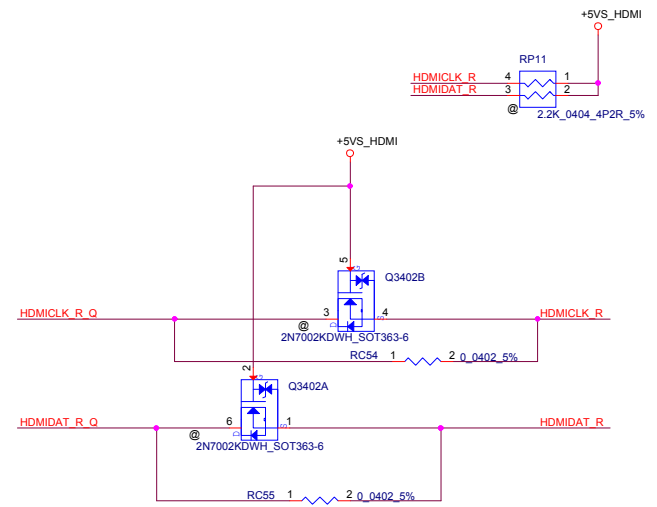
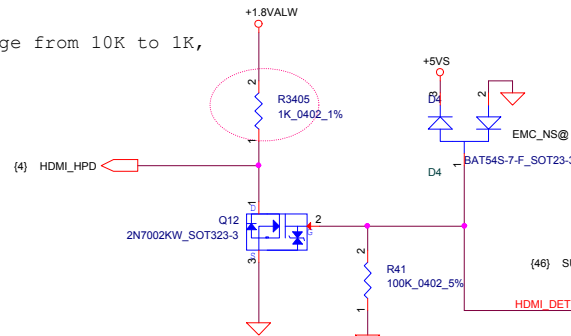


C23 0.1u for G HSW panel blink issue

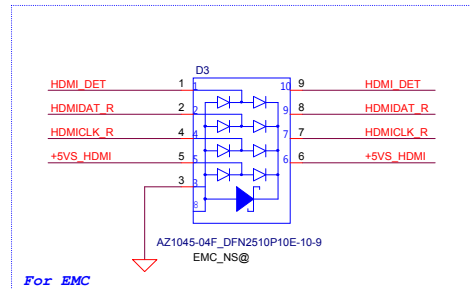
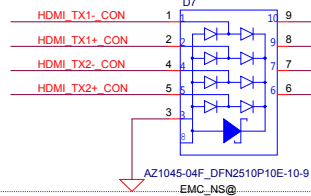
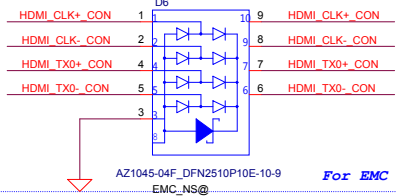





R4602 change from 10K to 1K,  
as Vienna



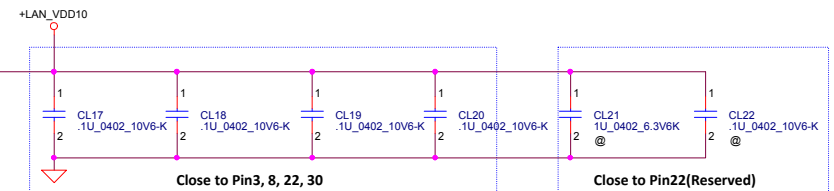
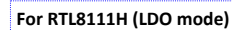
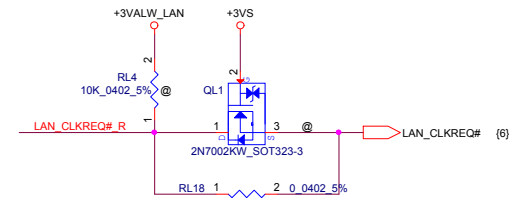
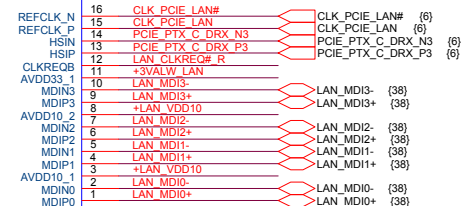
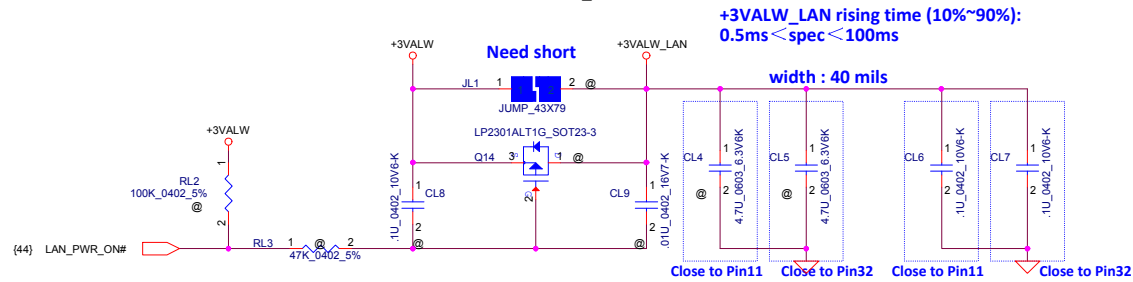
### Close to JHDMI1



Security Classification		LC Future Center Secret Data		Title			
Issued Date		2014/09/24		Deciphered Date		2015/03/23	
						HDMI_CONN	
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Date:		Tuesday, April 07, 2015		Sheet		34 of 60	



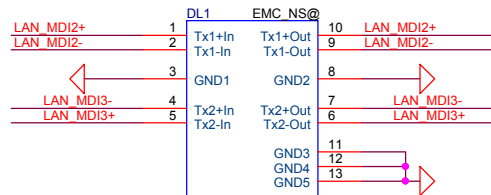




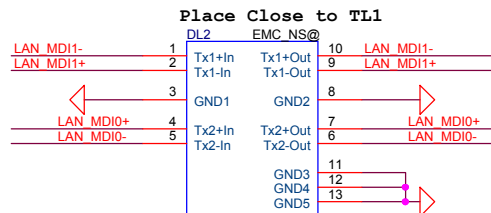
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil

Title		LAN_RTL8111GUL/RTL8106E		LCFC	
Size	Document Number	BMWC1		Rev	0.4
Custom		Date	Tuesday, April 07, 2015	Sheet	37 of 60

DL1/DL2  
1'S PN:SC400007R00

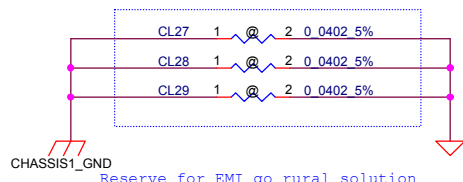


RCLAMP3374N.TCT\_SLP3020N10-10

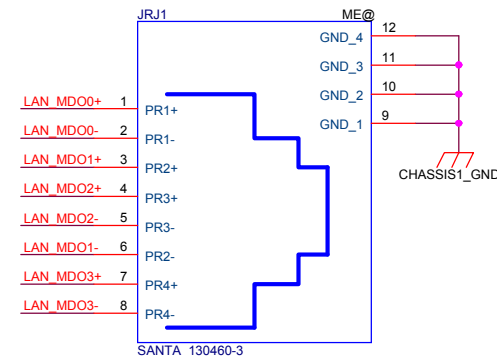
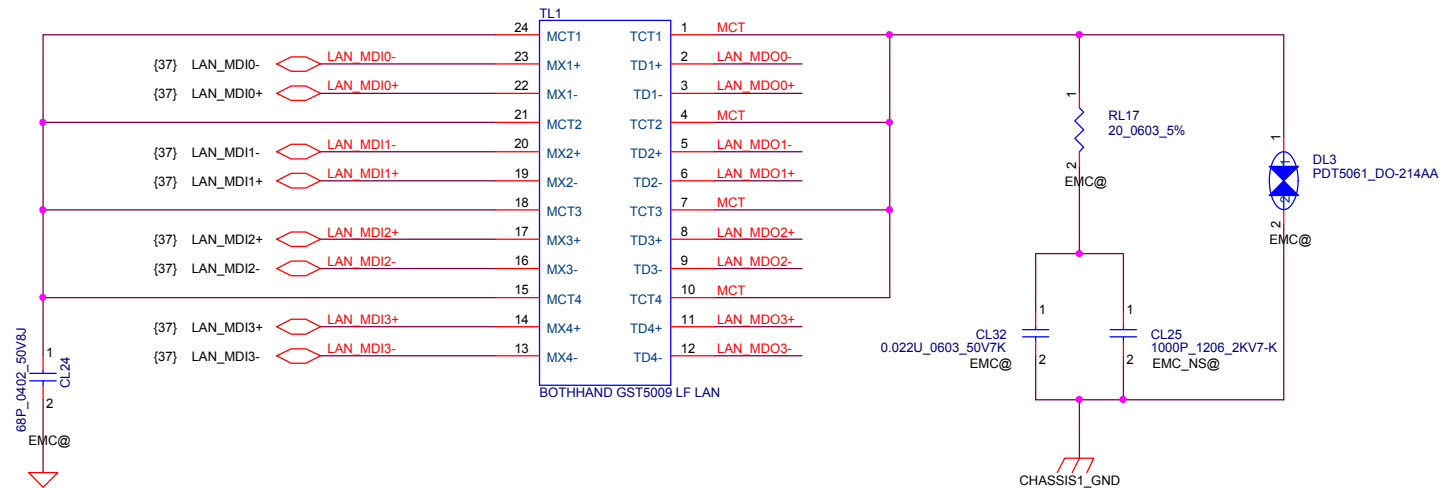


RCLAMP3374N.TCT\_SLP3020N10-10

Place Close to TL1

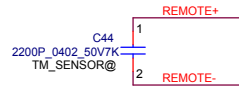


Reserve for EMI go rural solution



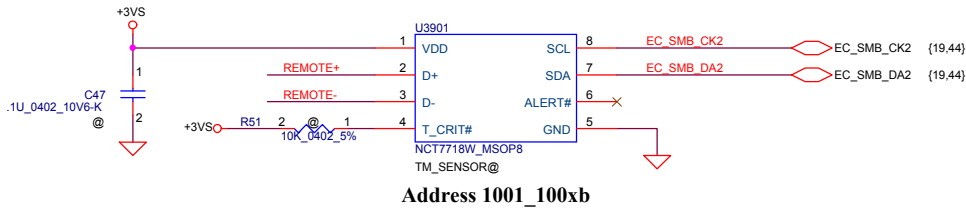
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	LAN_Transformer	
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				BMWC1	0.4
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## Close to U3901

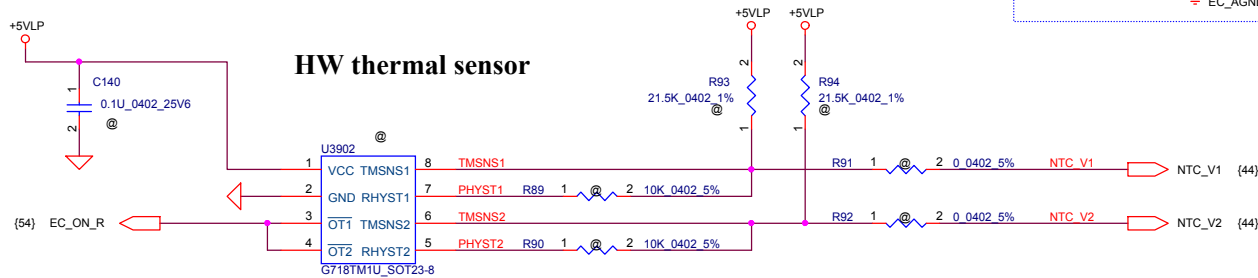


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

## SMSC thermal sensor placed near DIMM

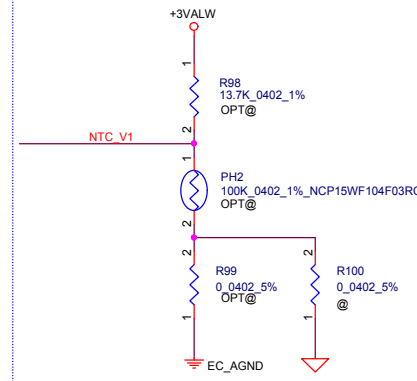


## HW thermal sensor

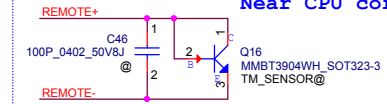


over temperature threshold:  
 $RSET = 3 * RTMH$   
92+/-30C  
Hysteresis temperature threshold.  
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$   
56+/-30C

## Near GPU&VRAM

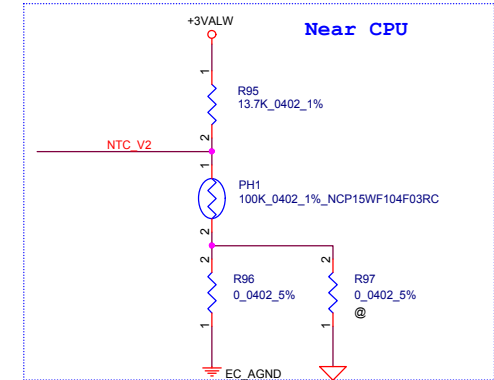


## Near CPU core

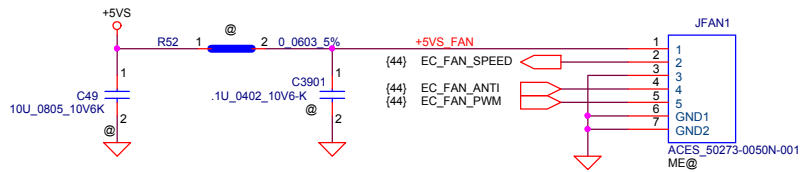


Baytrail SOC use thermal sensor to read the thermal,  
Baytrail don't has PECI signal


## Near CPU



## FAN Conn

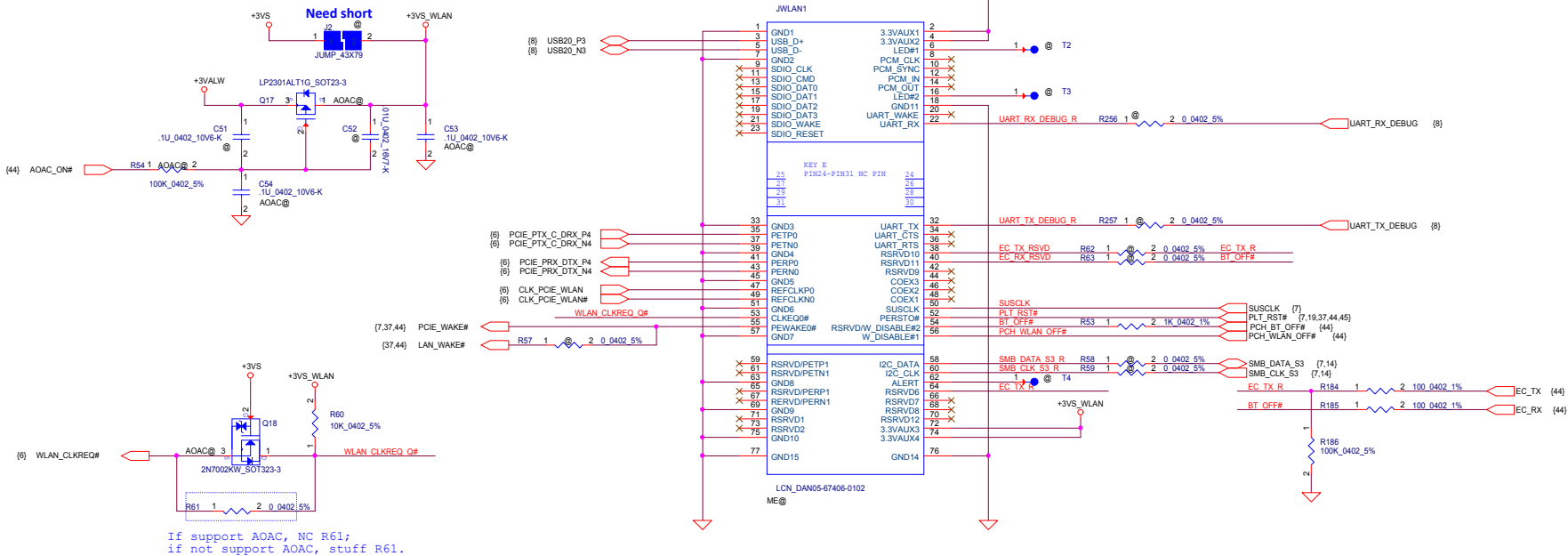


JFAN1 Pin defin need check other G

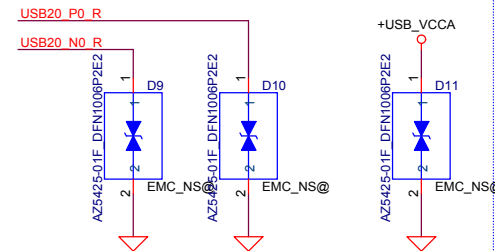
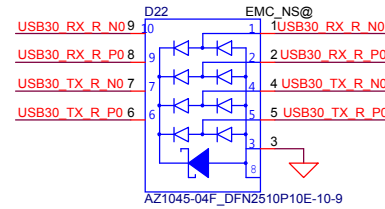
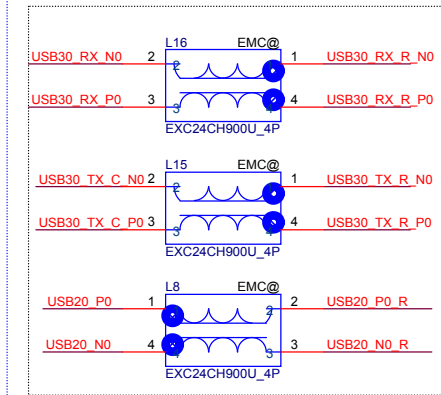
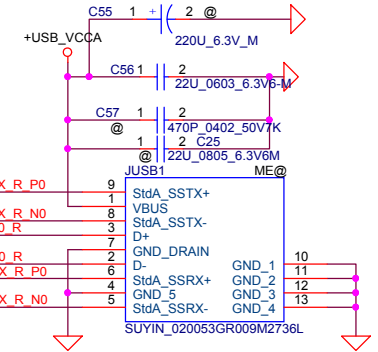
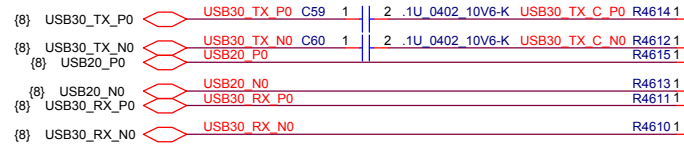
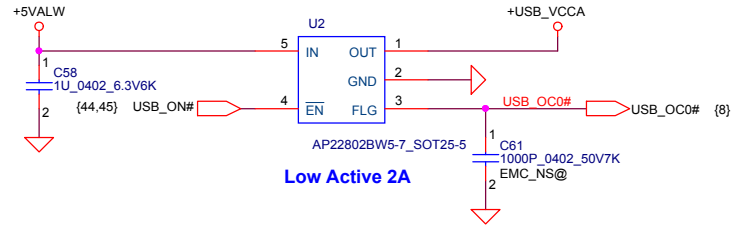
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	Thermal sensor/FAN CONN	
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					<div> Sheet 39 of 60 </div>



# Mini-Express Card(WLAN/WiMAX)




# LEFT SIDE USB3.0 PORT X1

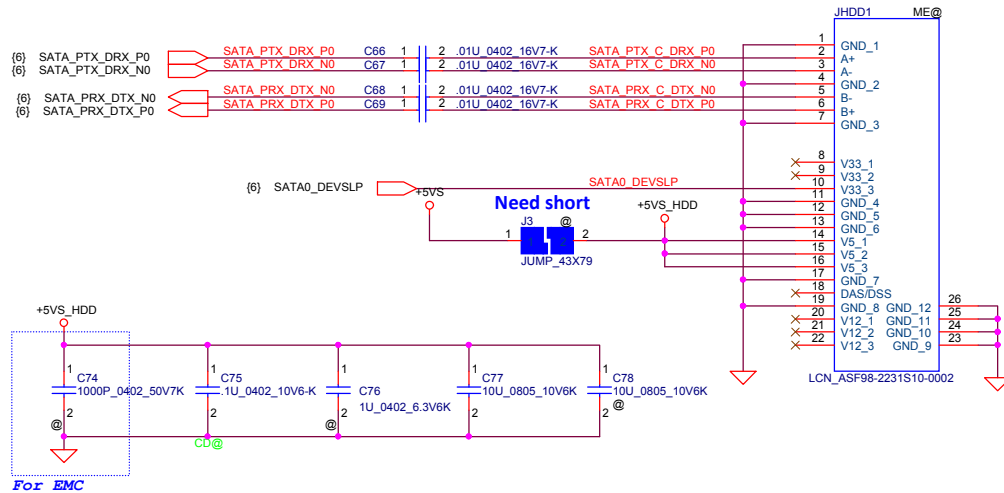


For EMC

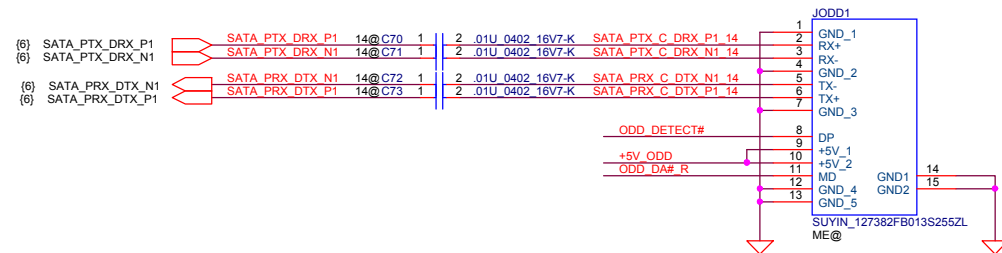
For EMC

Security Classification		LC Future Center Secret Data				Title					
Issued Date		2014/09/24		Deciphered Date		2015/03/23				USB2.0/USB3.0 PORT (LEFT)	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>											
Size		Document Number				Rev					
Custom		BMWC1				0.4					
Date:		Tuesday, April 07, 2015		ISheet		41		of 60			

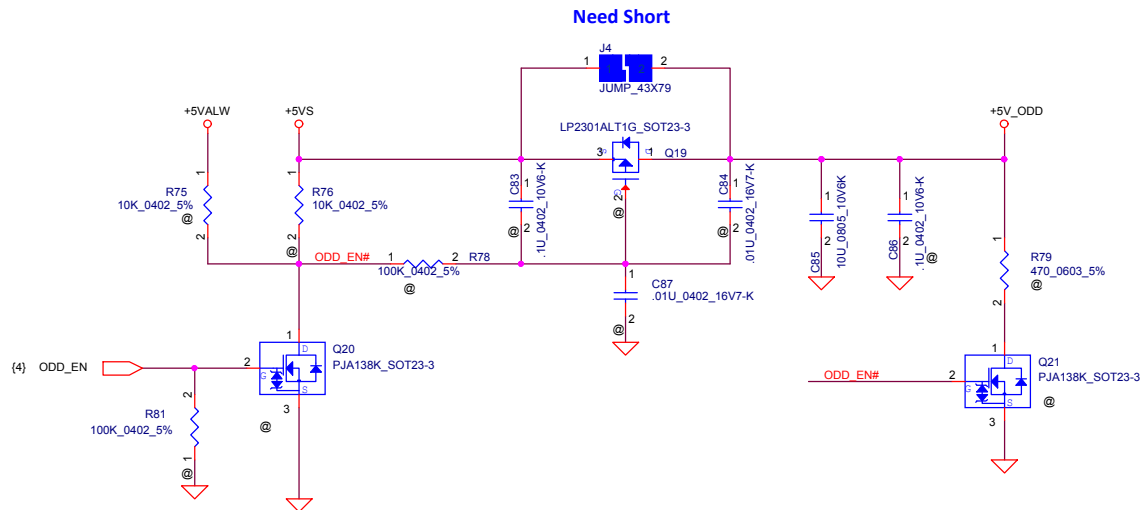
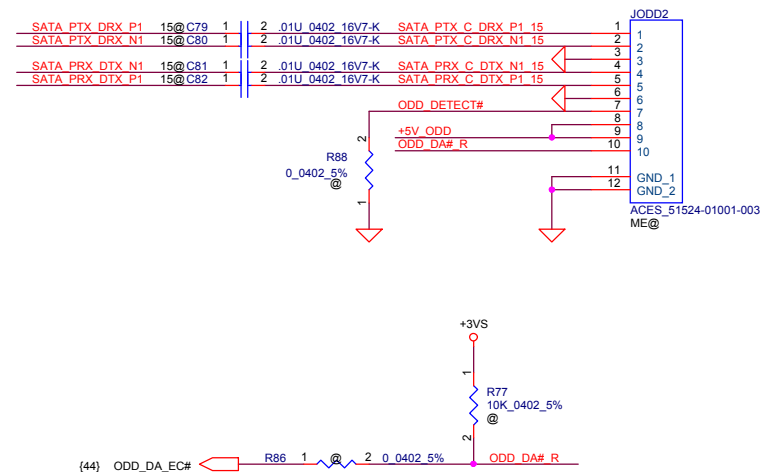
# SATA HDD Conn.



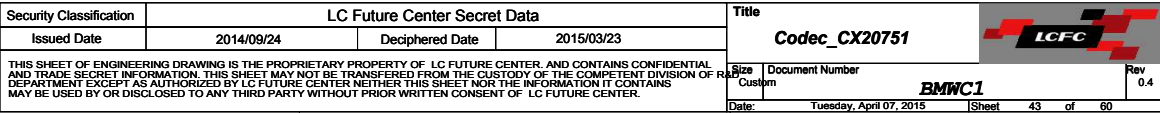
# FOR 14" SATA ODD Conn.

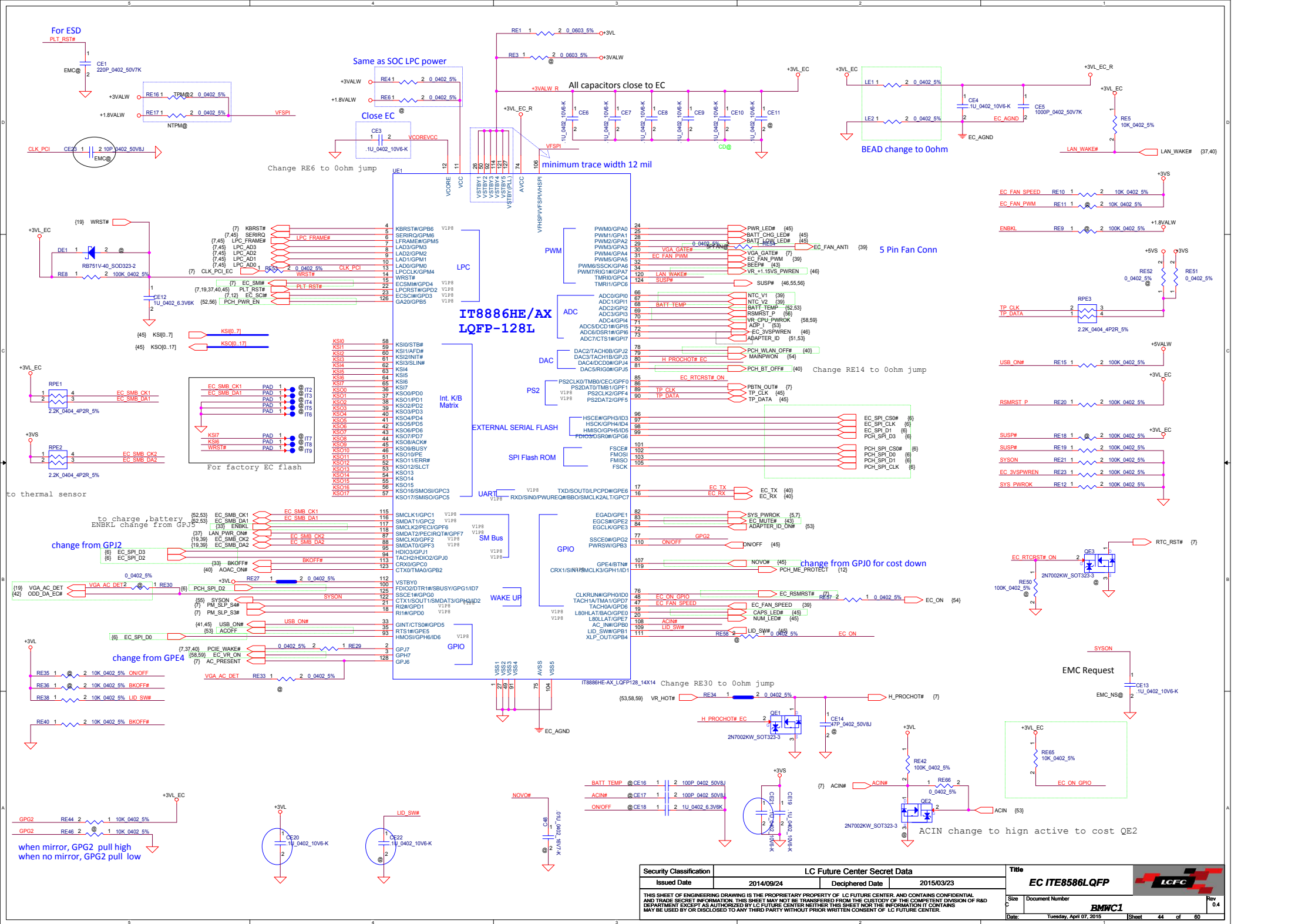



# FOR 15" SATA ODD FFC Conn



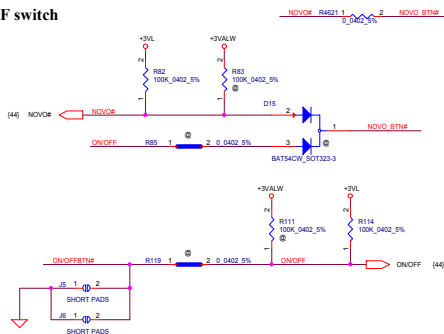
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	HDD/ODD CONN	
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Date: Tuesday, April 07, 2015				Sheet	42 of 60
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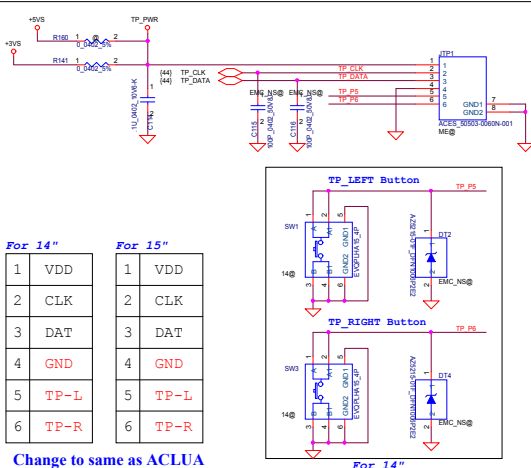


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2014/09/24		2015/03/23		Size		Document Number BMWC1	
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## ON/OFF switch



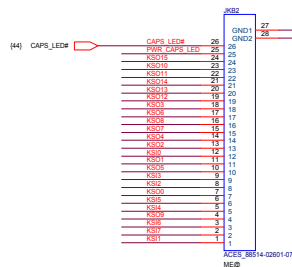
## TP/B Connector



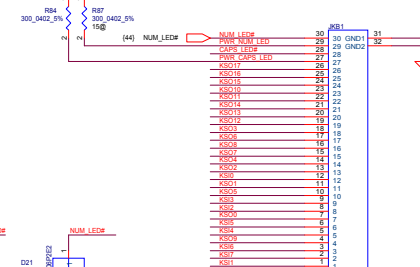
## K/B Connector



## 14"

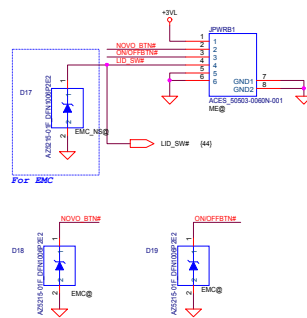


## 15"

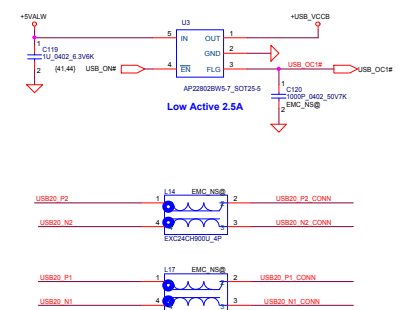


14"	15"
KB_1	KB11_14
KB_2	KB17_14
KB_3	KB16_14
KB_4	KB09_14
KB_5	KB14_14
KB_6	KB15_14
KB_7	KB00_14
KB_8	KB12_14
KB_9	KB13_14
KB_10	KB05_14
KB_11	KB01_14
KB_12	KB10_14
KB_13	KB02_14
KB_14	KB04_14
KB_15	KB07_14
KB_16	KB08_14
KB_17	KB06_14
KB_18	KB03_14
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KB_23	KB10_14
KB_24	KB11_14

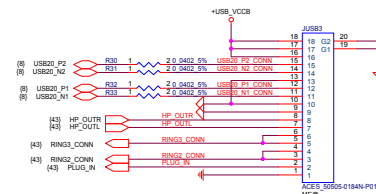
## PWR/B Connector



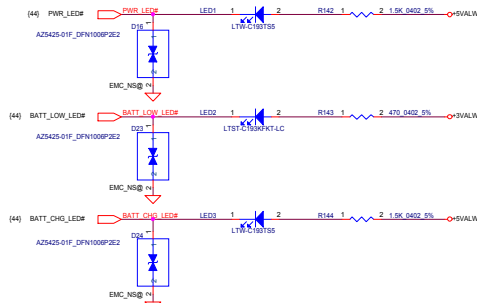
## Right Side USB2.0 Port X 2 (USB/B)



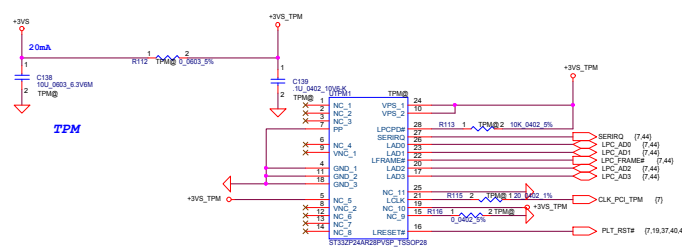
## USB I/O Connector



## LED



## TPM



Security Classification	LC Future Center Secret Data	Title
Issued Date	2014/09/24	Deciphered Date
2015/03/23		

Size	Document Number	Rev
0.4	0.4	0.4

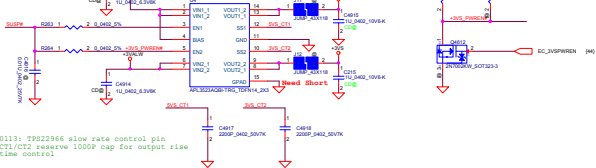
check LED location and BOM structure when placement and Load BOM, PWR, LED and BATT LED have the same location on 14"/15" 02/26

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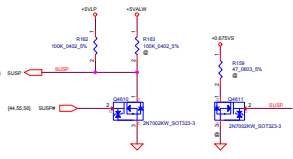
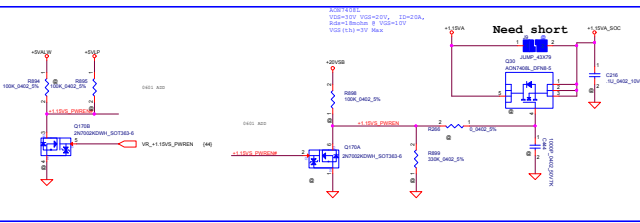
LCFC

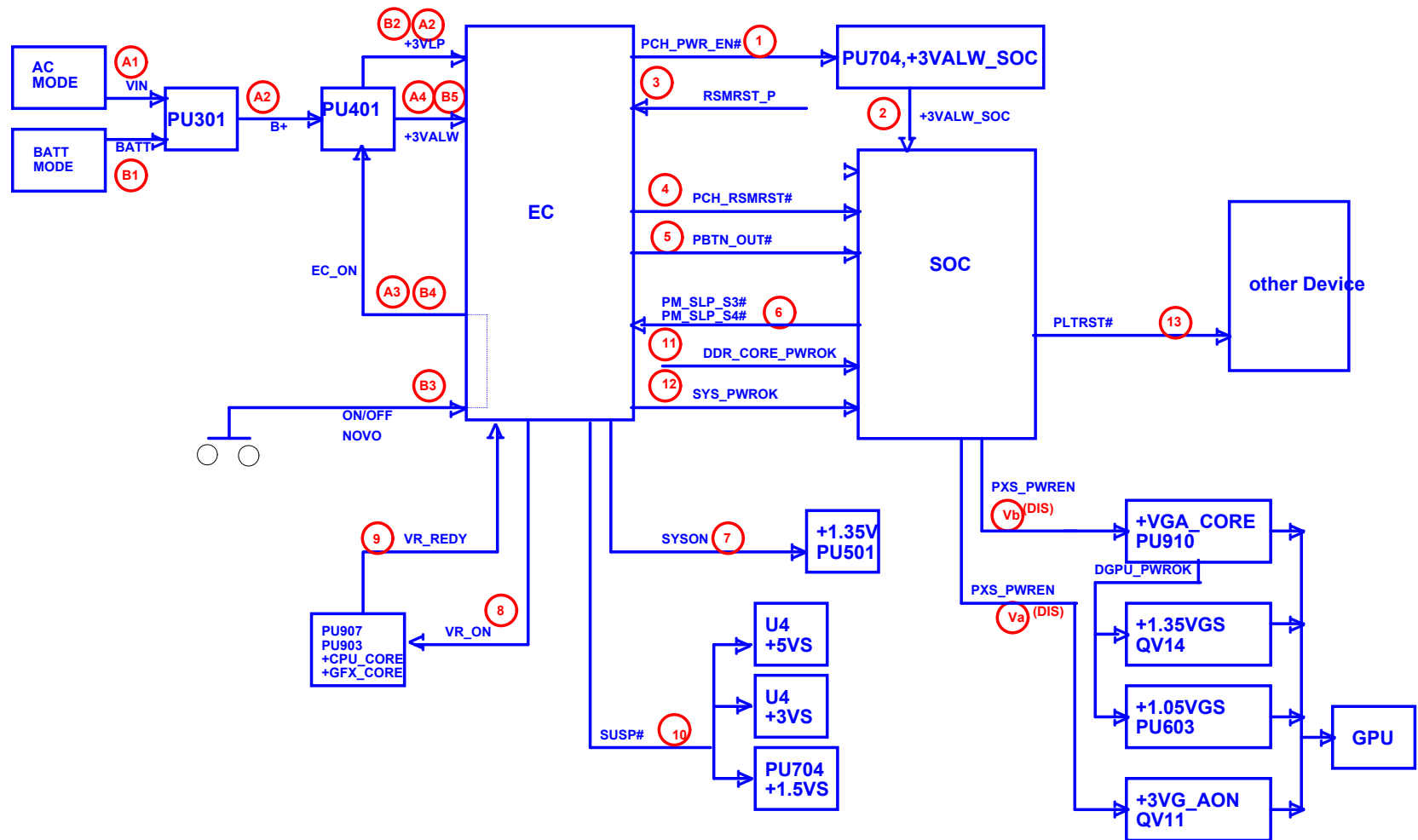
+5VALW to +5VS

+3VALW to +3VS

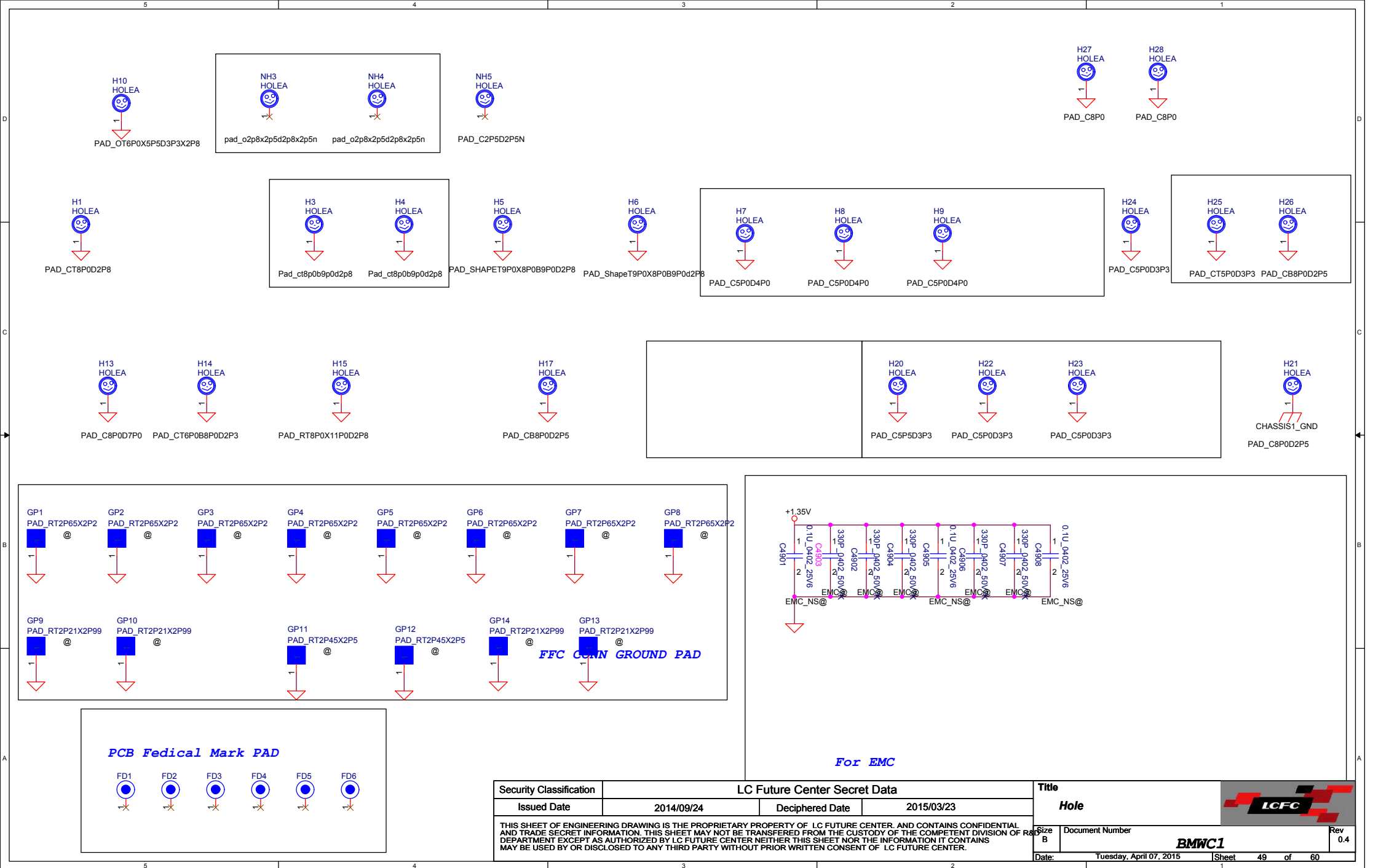


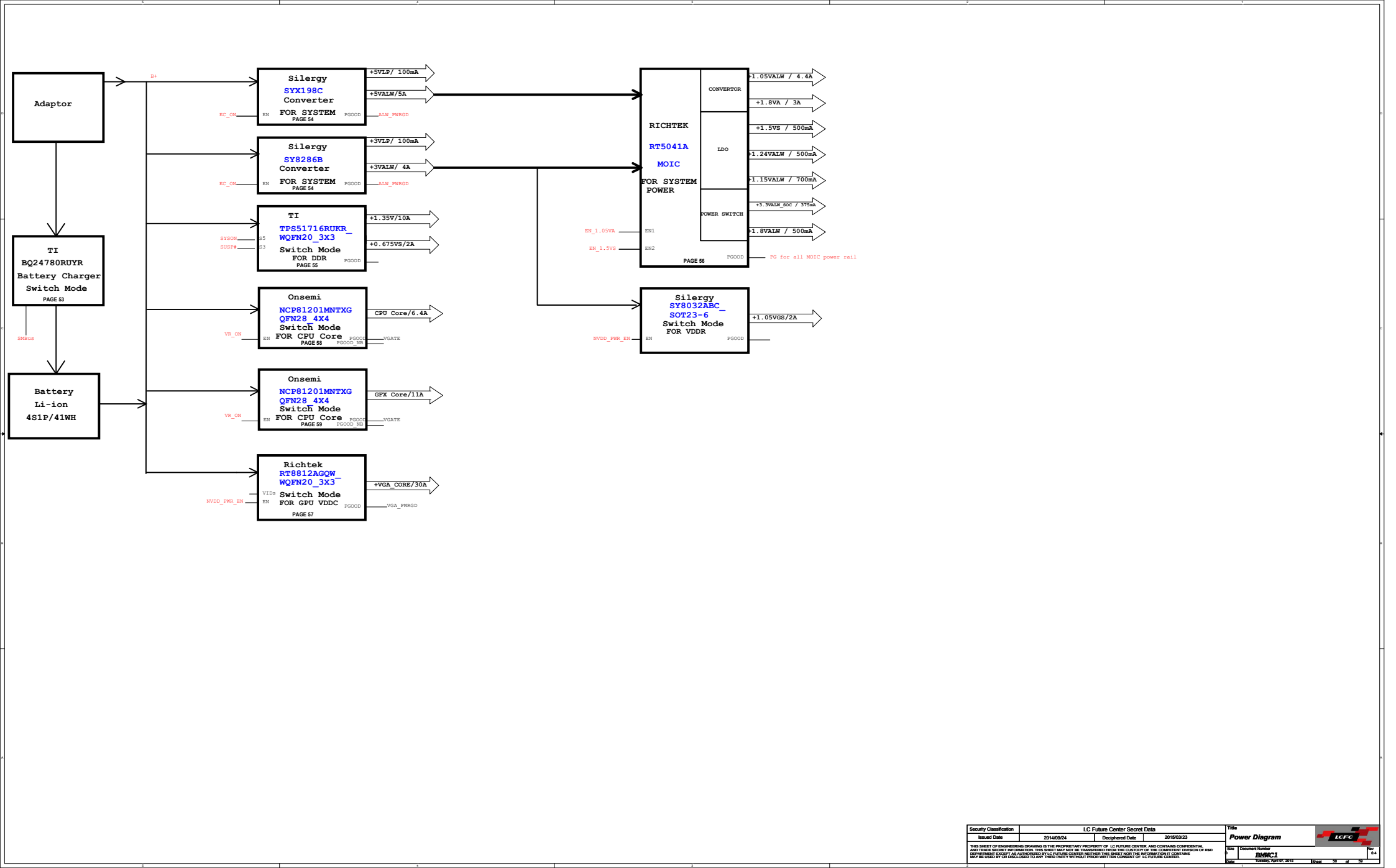
0113: TP222946 slow rate control pin  
CT1/CT2 reserve 1000P cap for output rise  
time control.

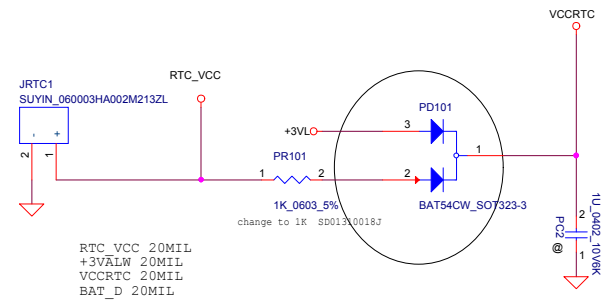
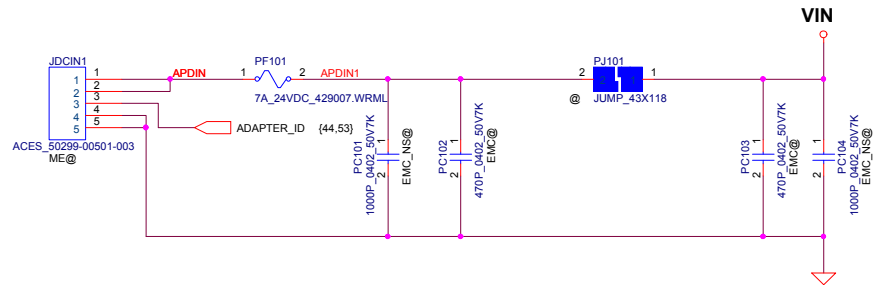


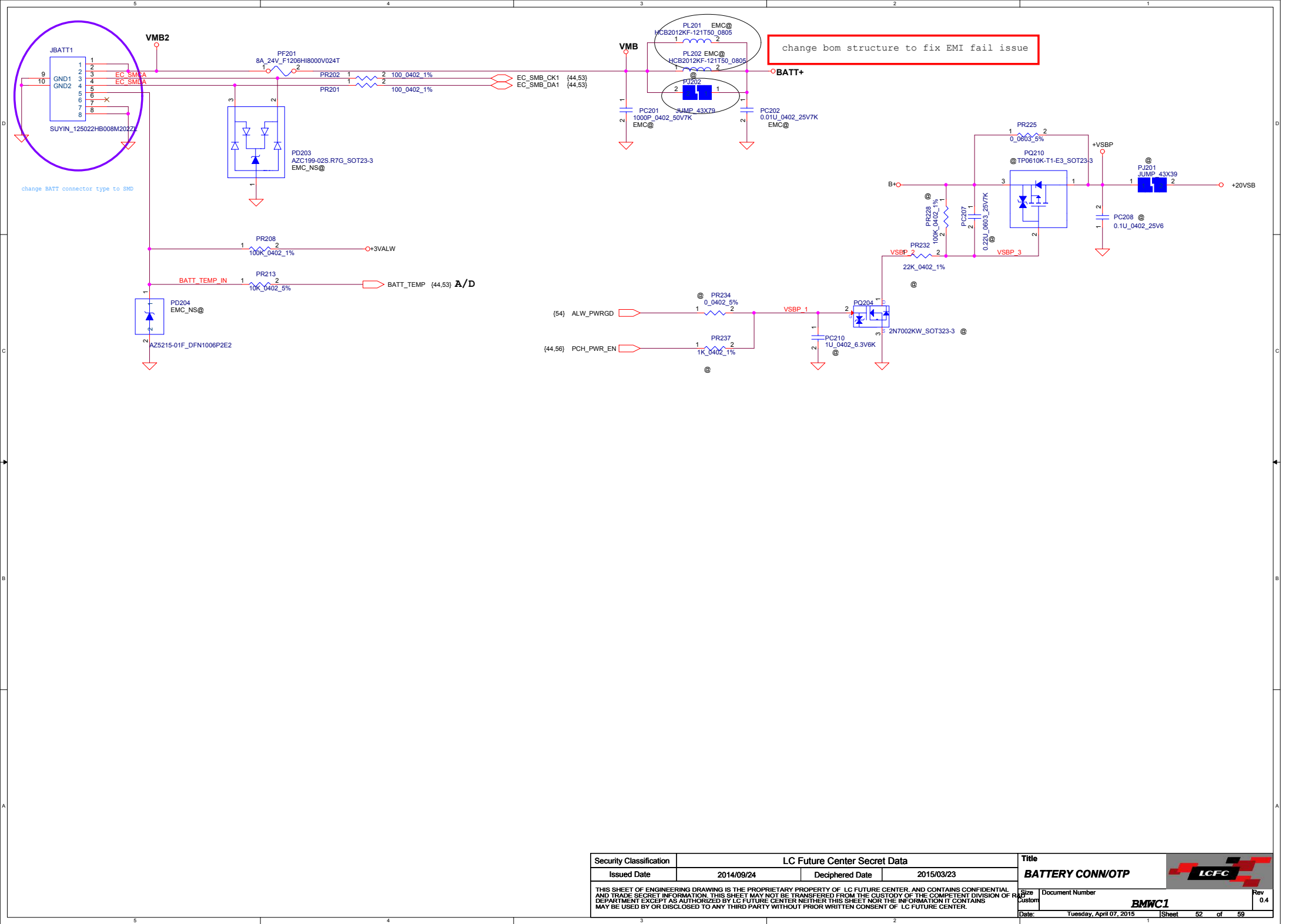




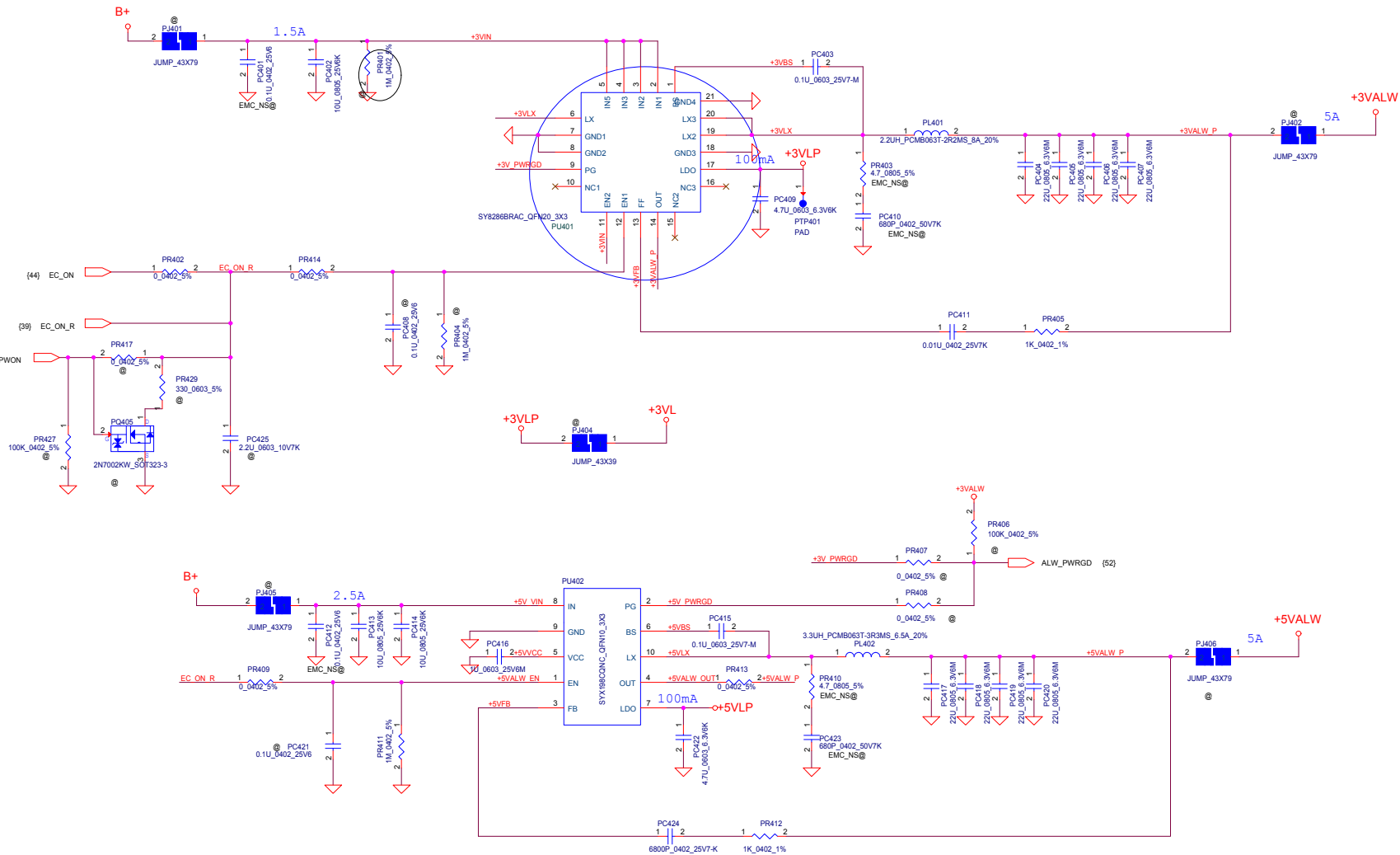


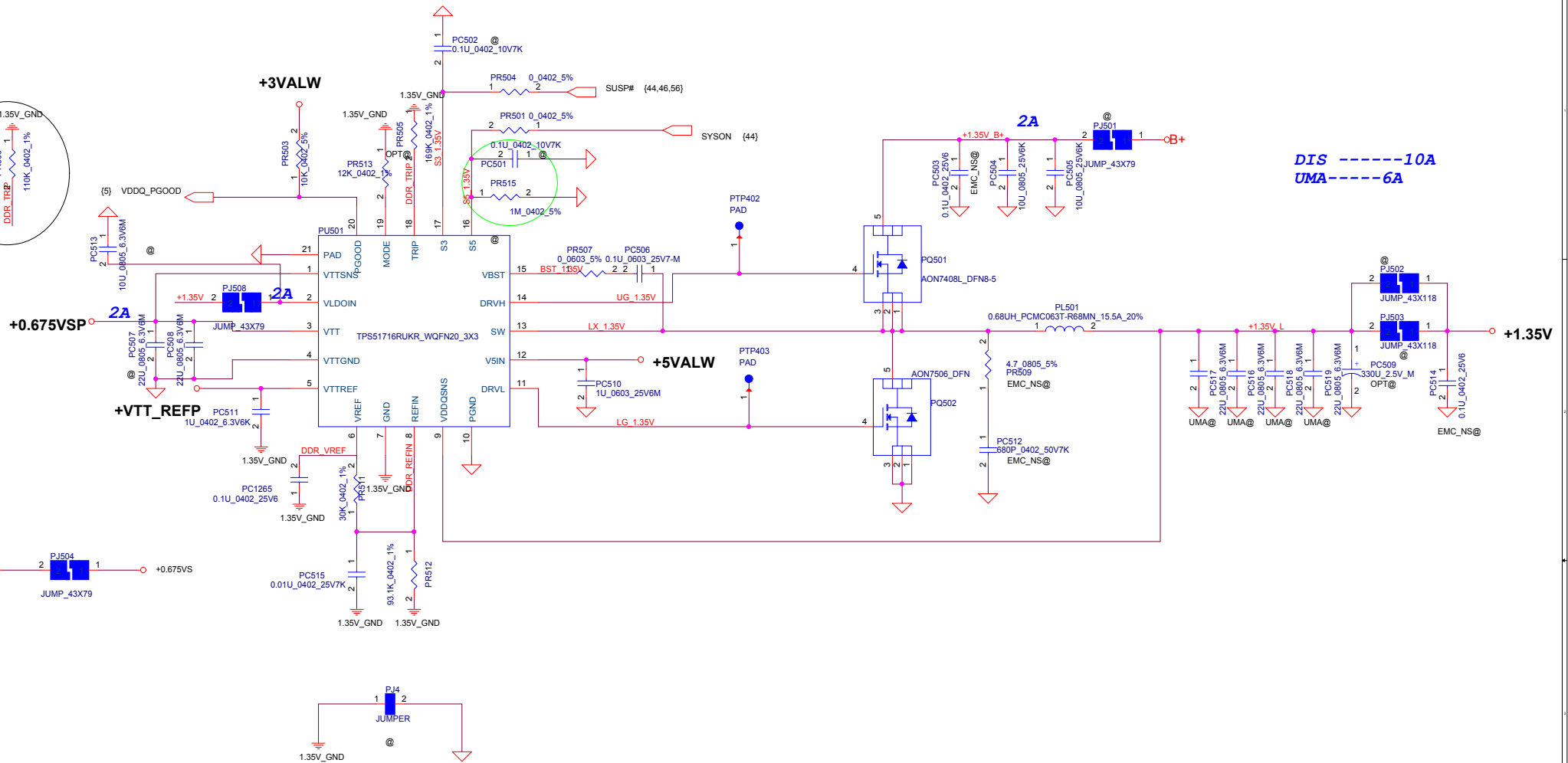
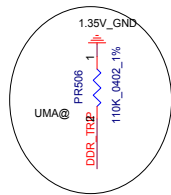












DIS -----10A  
UMA-----6A

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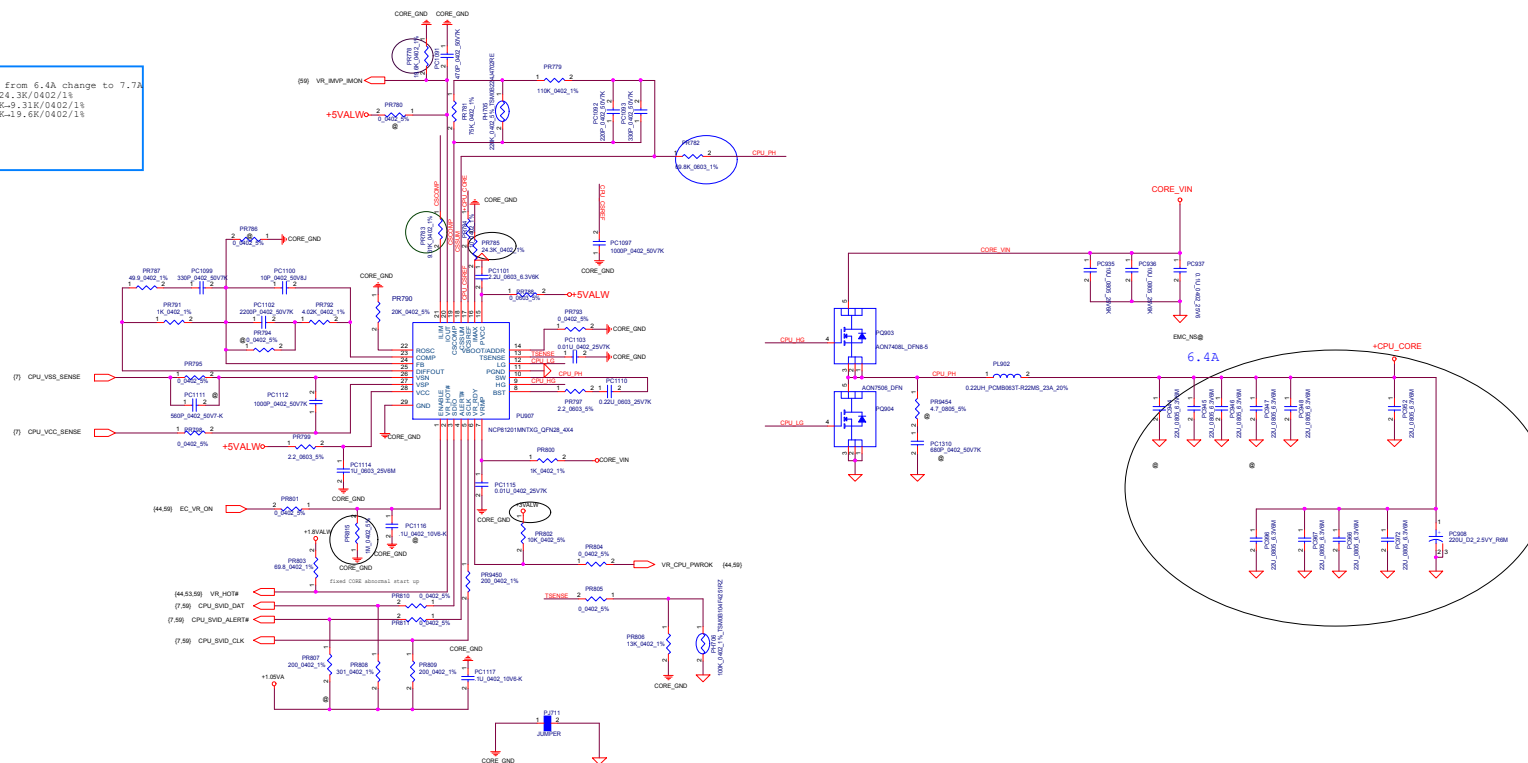
Title		1.35VS/+0.675VS	
Size	Document Number	BMWC1	
Date:	Tuesday, April 07, 2015	Sheet	55 of 59
Rev	0.4		







for CPU TDC from 6.4A change to 7.7A  
PR785: 21K-24.3K/0402/1%  
PR783: 7.68K-9.31K/0402/1%  
PR778: 20.5K-19.6K/0402/1%



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			Released By
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			Stamp
			Initials
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			Sheet Status
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			Sheet Attachments
			Sheet References
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			Sheet Properties
			Sheet Settings
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